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DESIGN OF HIGH SPEED VLSI ARCHITECTURE OF BRENT-KUNG ADDER USING QCA TECHNOLOGY

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ABSTRACT

In most digital circuit designs, including those for digital signal processors (DSP) and microprocessor datapath units, the binary adder is a crucial component. As a result, intensive research is still being done to increase the adder's speed. Parallel-prefix adders are known to perform the best in VLSI implementations.

One of the most crucial logic components in a digital system are binary adders. Additionally, binary adders are useful in Arithmetic Logic Units (ALU) as well as in other units like multipliers, dividers, and memory addressing. Therefore, binary addition is crucial because any advancement in binary addition can enhance the performance of any computing system, ultimately enhancing system performance as a whole.The most effective VLSI adders are known to be parallel-prefix adders. This study examines a majority-based Brent Kung adder, which uses less latency than a device that uses basic gates.The Xilinx-ISE tool is utilised in this project for simulation, logical verification, and further synthesising.

Brent Kung Adder, QCA Majority Gates, and VLSI Architecture are some key words.

1.INTRODUCTION

Quantum dot cellular automata, also known as QCAs, are hypothesised models of quantum computation that were developed in analogue to the traditional cellular automata models first proposed by von Neumann[1]. Information processing in nanoelectronic systems enters a new era of density and speed. has been created by the Notre Dame group.[1]The first actual suggestion for a technique based on networked quantum dot arrays is these "Quantum Cellular Automata" (QCA's). In the literature, it is referred to as the Notre Dame Logic Cell[1].], serves as the fundamental building element of these cellular arrays. The Coulomb exclusion phenomenon, which is a result of the interaction of quantum confinement Each cell exhibits a bi-stable behaviour as a result of the Coulomb interaction and this

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allows for the utilisation of the cells in large-scale cellular arrays[1]. Logic operations have been implemented by taking use of the physical interaction between adjacent cells. This allows for the creation of new functionality, and the University of Notre Dame team developed a flexible majority logic gate[1]. Boolean logic gates, inverters, crossed wires, and QCA circuits are all viable options. was shown in a number of papers[1]. One significant discovery is that all logic functions can be incorporated hierarchically, enabling the building of intricate QCA structures[1]. Majority Logic (ML): The ML action, represented by the notation M(x1,..., xn), serves as a voter, with n often being an odd number[2]. If greater The function will return the true value if more than [(n 1)/2] of the input variables are true.The majority-of-three function (see Fig. 1) is used to operate on the three boolean values A, B, and C. yields the logical expression as follows: [10]

$$F = M(A, B, C) = AB + AC + BC. \quad (1)$$

Any one of the three inputs can be used to simplify the majority-of-three function into AND or OR. constant value of zero or one[2][9]. M(A, B, 0) = AB and M(A, B, 1) = A + B, respectively. Hence M(A, B, 0) = AB and M(A, B, 1) = A + B, respectively. Hence, [9]Logic based on AND/OR can be considered as a generalisation of ML[2]. Recent developments have established When ML-based logic is used as a graph model for Boolean functions, the synthesis results for FPGA/ASIC and nanocircuit designs are good. [2].. XOR gates are frequently used in arithmetic circuits. [2]Two input XOR expressions call for three majority-of-three actions, or.

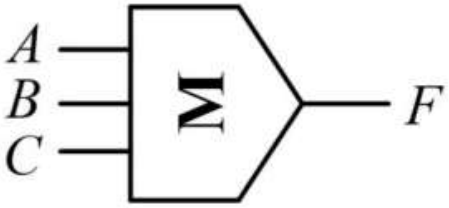

Fig. 1. Schematic of the majority gate.

2.LITERATURE SURVEY

CH. CURY MALOTHU KIRAN KUMAR " Using Quantum Computational Acceleration to Implement the Brent-Kung Adder"[1].One cutting-edge method for building Quantum-dot cellular automata (QCA) enables ultradense, low-power, and high-performance digital circuits. As transistor sizes go smaller, more and more of them may fit on a single chip, boosting the processing power of the chip[1]. Transistors, however, are limited to their current size. A basic component of a The cellular automaton built on quantum dots is a straightforward cell. Wires and gates can be built using the cell as a

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construction block[1]. One method for getting over this physical restriction is the QCA technique, or quantum-dot cellular automaton. In The novel Brent Kung adder (BKA) created in this study performs well and offers the optimal area-delay tradeoff.[1]. Dr. Neetesh Raghuwanshi, Dr. Bharti Chourasia, and Saket KumarThe phrase "Implementation of Vedic Multiplier Using Brent Kung Adder Technique" [3]The thesis of this research paper is major goal is to build an architecture for a sophisticated Vedic multiplier by fixing flaws in the current approach and enhancing speed by employing the Brent Kung adder with the aid of the hybrid square technique[3]. Ordinary multipliers work well for lower order bits, while the Vedic multiplier technique is typically employed for situations requiring greater bit lengths[3].Ali Ahmadian, Ferial Ghaemi, Norazak Senu, Jadav Chandra Das, Debashis De, and Sankar Prasad MondalIn 2019, IEEE published "[8] "QCA Based Error Detection for Nano Communication Network" (volume 7, number 7). [8]In this research, we present the design of low-power nano-scale circuits for even Quantum-dot cellular automata (QCA)-based parity generator and checker circuits.A new method of generating and verifying even parity has been proposed. XOR gate configuration. [8]This new XOR gate is significantly quicker and more dense than its predecessors.

3.EXISTED DESIGN

BRENT KUNG ADDER

The parallel prefix adder is a type of calculator. The usage of produce and propagate signals forms the foundation of the specific class of adders known as parallel prefix adders.Because of their adaptability, these are employed to handle binary additions. [6]Keep Looking Forward The parallel prefix adders is obtained by employing the Adder's (CLA) structure. The technique for tree structures is used to accelerate mathematical operations.

There are There are three steps in creating a parallel prefix adder:

1. The preliminary stage:This stage involves computing the signals that are generated and propagated to each pair of inputs A and B.

Pi = Ai xor Bi

Gi = Ai and Bi

2. Carry generation network:[5Each bit has its associated carry set at this time. determined. These actions are all implemented and completed concurrently.After the stage has been implemented, parallel carries are separated into pieces.Carry, propagate, and generate. signal intermediaries. that the logic equations provide[7]:

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CPi:j = Pi:k+l and Pk:j

CGi:j = Gi:k+l or (Pi:k+l and Gk:j)

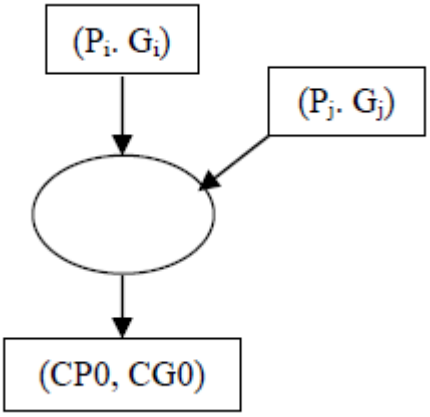

Fig2:Carry network

3. Stage 5 of the Carry Network Post Processing:The summing of the input bits is computed in this final step.

Ci-1= (Pi and Cin)

Si =Pi xor Ci-1

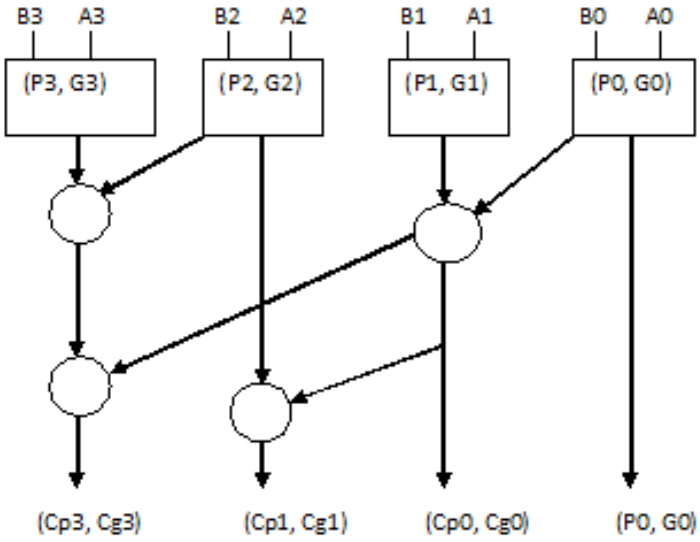

Fig3: 4-bit Brent-Kung adder

4.PROPOSED DESIGN

BRENT KUNG ADDER USING MAJORITY LOGIC

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In order to In high-performance To improve performance, adders and parallel prefix adders are used. operation speed.However, the Brent Kung Adder's (BKA) numerous levels slow down its performance[4]. Due to its lowest area delay and high input bit count, BKA is also power efficient [4] The "o" operator has log2n x 2 stages, which is the BKA delay. The BKA has a coverage area (the number of "o" operators) of where n is the total amount of input bits. (2*n)-2- log2n [4]. The BKA is renowned for having a high logic depth and a small footprint [4]. Here, a high fan-out characteristic denotes a high logic depth[4].

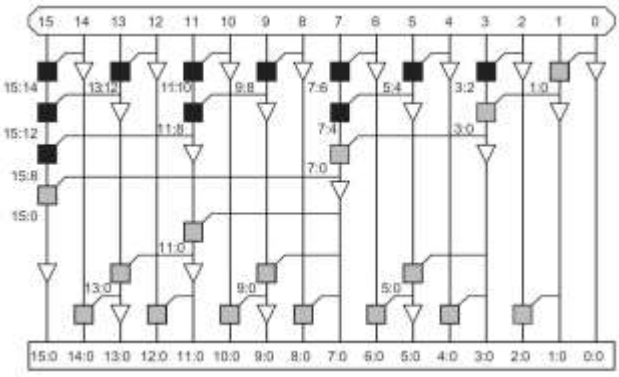

Fig 4 : 16-bit Brent Kung Adder

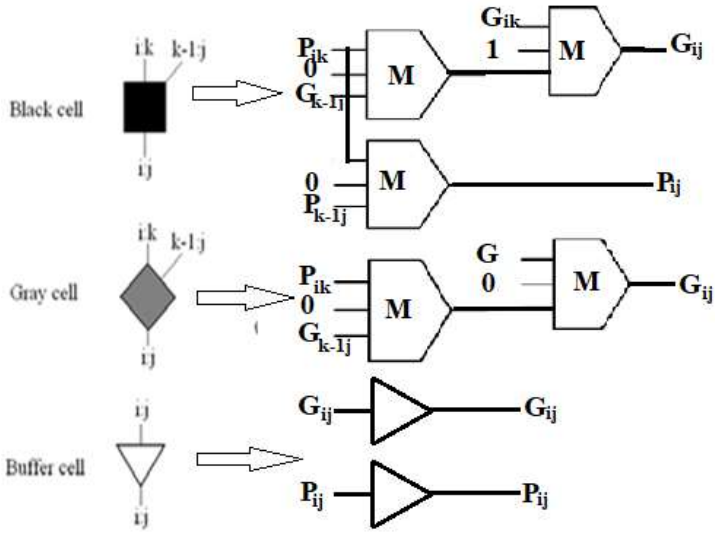

Fig 5:Complex logic cells inside the Prefix Carry Tree using Majority logic

5.RESULTS

RTL Schematic: Register transfer level, also known as RTL, is an acronym for the blueprint of the architecture. It is used to compare the designed architecture to the yet-to-be-created ideal

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architecture.Using the coding languages i.everilog and vhdl, the hdl language translates the architecture's description or summary into its working summary. To facilitate analysis, even the internal connection blocks are specified in the RTL schematic.The image below depicts the RTL schematic diagram of the designed architecture.

Fig6:Proposed RTL schematic view

Technology SchematicThe technology schematic in the LUT format, which uses the LUT as the parameter of area to estimate the architecture design in VLSI, serves as a representation of the architecture.There are LUTs in FPGA that reflect the memory allocation of the code, and the LUT is thought of as a square..

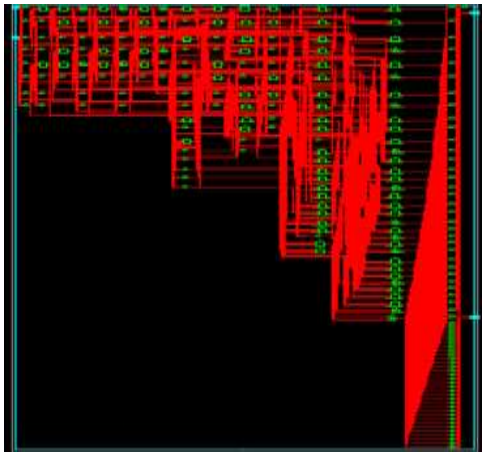

Fig7: Proposed techonology schematic of bka

Simulation: Simulation is the procedure, whereas the schematic is used to verify the connections and building components. The simulation window is activated on the tool's home interface as the tool transitions from implantation to simulation. The simulation output is limited to wave forms by the simulation window. This is adaptable enough to offer numerous radix number systems

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Fig8: Proposed simulated wave forms

Parameters: Area, latency, and power are three variables that are considered in VLSI; using these variables, one can compare one architecture to another. Here, a parameter that takes into account delay is obtained using the XILINX 14.7 tool, and verilog is the HDL language.

Parameters	Existed 32-bit BKA	Proposed 32-bit BKA
Delay(ns)	19.643	17.830

Table 1: Parameters comparison

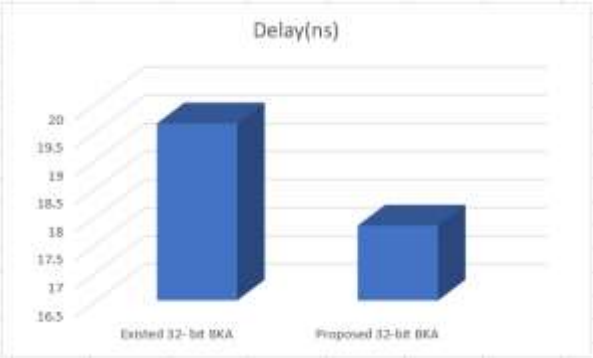

Fig9: Delay comparison bargraph

CONCLUSION

The implementation and high-performance analysis of a 32-bit Brent KungAdder with QCA majority gates is shown in this research.The experimental results show that the suggested adder succeeds in achieving its original goal of providing an unbiased optimised outcome of delay without compromising accuracy. The simulation results are shown in the Xilinx ise design suit. Additionally, it was discovered that the evaluated application's quality requirements had not been compromised.

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