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Low power VLSI Architecture of Adaptive Recursive Karatsuba Multiplier with SquareRoot-Carry-Select-Adder using Reversible logic

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ABSTRACT

Nowadays, fast binary multiplication is necessary for computationally intensive applications like DSP, image processing, floating point processors, and communication technologies. This block often consumes the most power and time. In order to cut down on time, this study suggests an effective architecture for unsigned binary multiplication. Reversible logic has been used to create a 1616-bit multiplier based on the Vedic Karatsuba algorithm. It is optimised utilising a square-root-carry-select-adder in conjunction with an adaptive and recursive technique. The designs were created using Xilinx ise and Verilog coding.

Key words—Square Root Carry Select Adder, reversible logic, Karatsuba Multiplier, Recursive Adaptive KaratsubaAlgorithm.

1.INTRODUCTION

One of the oldest methods the Aryans utilised to conduct mathematical computations is Vedic Mathematics. This consists of formulas that can reduce complicated mathematical processes to quick mental calculations[1]. The aforementioned benefit results from Vedic mathematics' completely unique methodology, which is also thought to be rather similar to how the human mind functions. It is important to recognise and appreciate Jagadguru Swami Sri Bharati Krishna Tirtha Maharaja's endeavours to teach Vedic Mathematics to laypeople and organise Vedic Algorithms into 16 Sutras[1]. One example is the

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Vedic algorithm. Such a multiplication algorithm is renowned for its effectiveness in minimising the number of calculations required.The most crucial design goals for integrated circuits are size and speed.Adders are one of the most common components utilised in the creation of digital integrated circuits. circuits because adding is the fundamental function of all computer arithmetic[8]. The design of efficient adders must take propagation of carry into account, hence this study proposes fast adders and analyses their performance[8]. Adder with Square Root Carry Selection (SQCSA) considered, offers an excellent balance between price and performance[8].

There is a growing demand for embedded and transportable Digital Signal Processing (DSP) systems as a result of advancements in VLSI technology[4]. In practically every field of engineering, DSP is prevalent. The current trend is for addition and multiplication to happen more quickly. The most fundamental and widely utilised operation on a CPU is multiplication[4]. The act of multiplying involves dividing one integer by another. Convolution, the Discrete Fourier Transform, the Fast Fourier Transform, and similar sophisticated procedures. all have their roots in multiplication operations. Faster arithmetic units are essential due to the constant demand for faster clock frequencies[4]. In order to implement new algorithms, DSP experts are continuously looking for new hardware. Multiplication can be done here with the help of Vedic mathematics.

2.LITERATURE VIEW

M. Bala Murugesh, S. Nagarraj, and J. Jayasree, IEEE Transactions on Circuits and Systems, Using the vedic method, "Modified High Speed 32-bit Vedic Multiplier Design and Implementation", vol. sutras of classical vedic mathematics, The binary vedic multiplier's modified version is described in the proposed study..It provides an adjustment to the initially established Multiplier Vedic.The binary vedic multiplier has been adjusted. recommended due to its enhancements in device utilisation and delay time.[3]The system was created and implemented using Verilog HDL. proposed approach.For HDL simulation, Modelsim is used, whereas Xilinx is used for circuit synthesis.Simulations for multiplication operations using bits of 4, 8, 16, and 32 have been performed[3]. "Anamika and Rockey Bhardwaj's article, "Reversible Logic Gates and Their Performances,"According to [6], a major problem with VLSI circuits is heat. IEEE Transactions on Circuits and Systems article by "Modified High Speed 32-bit Vedic Multiplier Design and Implementation", a paper by M. Bala Murugesh, S. Nagarraj, and J. Jayasree, was published in vol. The changed form of the binary vedic Classical vedic mathematics sutras are used to explain the multiplier in the suggested study project.It changes the way the Vedic Multiplier was set up in the beginning.It is suggested to use the adjusted binary vedic multiplier because it

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improves how well devices work and how long it takes to do something.[3]Verilog HDL was used to make the suggested method and put it into action.Xilinx is used to put together circuits, while Modelsim is used to model HDL.Simulations have been made of how to multiply with 4, 8, 16, and 32 bits. "Reversible logic gates and its performances" was written by Anamika and Rockey Bhardwaj.According to [6], one of the biggest problems with VLSI systems is heat.

3.EXISTED DESIGN

VEDIC MULTIPLIER USINGKARATSUBA MULTIPLICATION ALGORITHM

Recursive Karatsuba is based on continually adding the When the bit size is large, the Karatsuba algorithm is used at each stage to improve speed [2]. Before The algorithm By applying the Karatsuba technique to the segmented bits repeatedly, the number of bits (N) is divided into groups of half the number of bits (N/2). For a 16-bit multiplication, the output is split into 8-bit multiplication, 4-bit multiplication, and then 2-bit multiplication, which is the final step before a standard multiplication. [2]We put flexible Karatsuba into place at each stage of the third product term.

Standard KaratsubaMultiplier

Consider X and Y to be 'n'-bit inputs. XH and XL and YL stand for lower order bits, while YH stands for higher order bits [2]. Their profit is calculable:

$$XY = \left(2^{\frac{n}{2}}X_H + X_L\right)\left(2^{\frac{n}{2}}Y_H + Y_L\right)$$
$$= 2^n(X_HY_H) + 2^{\frac{n}{2}}(X_HY_L + X_LY_H) + (X_LY_L) \qquad (1)$$

The computation is revised as follows in Karatsuba algorithm:

$X_HY_L + X_LY_H = (X_H + X_L)(Y_H + Y_L) — X_HY_H — X_LY_L$(2)

Thus, multiplications involving 4n/2 bits can be boiled down to 3n/2 bits. multiplications:$(X_H+Y_H)(X_L+Y_L)$,$X_HY_H$and X_LY_L.Figure.1 demonstrates the standard Karatsuba multiplier for n-bit inputs.The traditional way to do multiplication takes a lot of time.:

$O(n)=n^2$ (3)

Karatsuba multiplication method, on the other hand, needs:$O(n)=n^{1.58}$ (4)

where O denotes the order of difficulty, 1 denotes O(1), and n is the number of bits. Because of the logarithmic power of n[2], this demonstrates analytically how much speedier the Karatsuba algorithm is

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than conventional multiplication. and its complexity of n1.58.

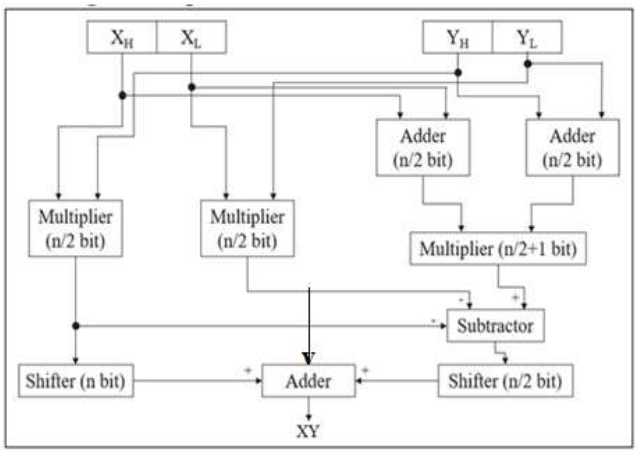

Figure. 1. Standard Karatsuba Multiplier for n-Bits

4.PROPOSED DESIGN

VEDIC MULTIPLIER USING KARATSUBA MULTIPLICATION BY ADAPTIVEALGORITHM USING REVERSIBLE LOGIC

The Karatsuba algorithm[2] is modified to make making it easier to figure out the third result. Assuming that both X and Y are 'n' bits, and the argument is the third product of (n/2 + 1) bits.LetZandUbethese arguments, leaving (n/2-1) bits behind. Because ZH and UH are the third product arguments, they represent the higher order bits, while ZL and UL represent the lower order bits.

(X_H+ Y_H) and (X_L+Y_L). Thus

$$\begin{aligned} \text{Product}_3 &= ZU \\ &= \left(2^{\frac{n}{2}}Z_H + Z_L\right)\left(2^{\frac{n}{2}}U_H + U_L\right) \\ &= 2^n(Z_HU_H) + 2^{\frac{n}{2}}(Z_HU_L + Z_LU_H) + (Z_LU_L) \quad (5) \end{aligned}$$

Based Table 1 displays the results of evaluating the aforementioned expression on ZH and UH.

THIRD PRODUCT COMPUTATION

Z_H	U_H	Product_3
0	0	Z_LU_L
0	1	$2^{\frac{n}{2}}Z_L + Z_LU_L$
1	0	$2^{\frac{n}{2}}U_L + Z_LU_L$
1	1	$2^n + 2^{\frac{n}{2}}(U_L + Z_L) + Z_LU_L$

Table 1

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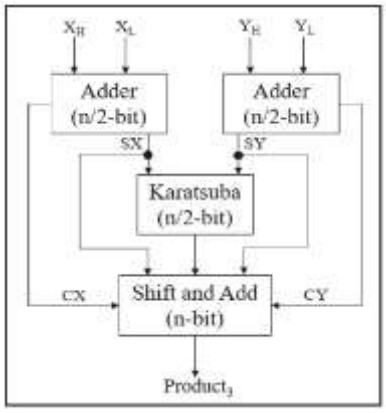

Figure. 2. Adaptive Concept for 3rd Product Computation

As seen in Table I, a computation involving the third product, which involves multiplying the (n/2 + 1) bits, requires one multiplication of the (n/2 -1) bits as well as extra shifting, adding, and multiplexing operations[2].Karatsuba implementation becomes recursive as a result, without requiring additional hardware. With n-bit inputs and Figure 2 shows the "Shift and Add" block in place., an adaptive approach to (n/2 + 1)-bit computation can be implemented. is used as necessary, as noted in Table I[2].

SQUARE ROOT CARRY SELECTADDER

Each sector of Two additions are performed simultaneously by the Square Root Carry Select Adder (SRCSA)[5,9], one with the carry-in assumed to be zero and the other with the carry-in assumed to be one within the sector[9].The block sizes are as follows: flexible. For the sake of conciseness, the entire analysis is not included here, however, for example, Alternate block sizes of 2-2-3-4-5, rather than the standard 4, can be used to build a 16-bit adder[2]. When When the Full-Adder and MUX delays are equal, this partition works well.[2][5]. In Figure 3, the block diagram of the proposed 16-bit SRCSA adder shows inputs A and B, carry-in designated by Cin, and outputs denoted by sum (S) and carry-out (Cout)[2].

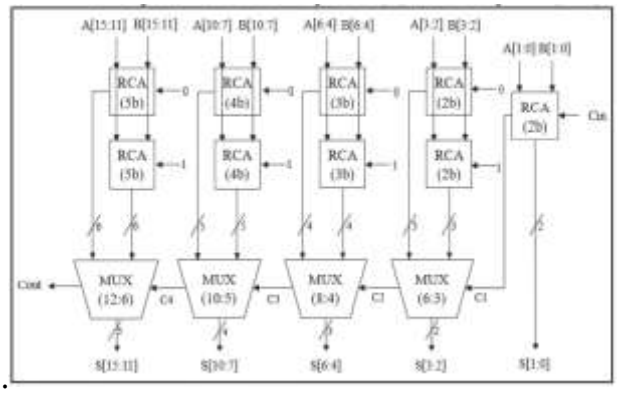

Figure. 3. 16-bit SRCSA (proposed adder)

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High performance and straightforward architecture function circuits have been built using Vedic methods. Banalization, however, frequently led to Due to conversion-hardware overhead, there is a trade-off between speed and simplicity in architecture, as many are based on the use of decimal numbers. However, due to creative circuit realisation, primarily multipliers, interest in Vedic algorithms has recently been rekindled. The current project is notable because it incorporates an adaptive element that enables recursive operations to lower the complexity ranking bit lengths range from square to logarithmic powers. which is a well-known algorithm (Karatsuba)[2].

REVERSIBLE GATES

chips with high performance How much we can actually boost system performance is constrained by the release of enormous amounts of heat[10]. The only physically viable means of continuing to improve performance will soon be Information is conserved in reversible circuits that uncompute bits rather than discarding them. Reversible computing will also increase the energy efficiency[10].As a result due to its ability to decrease electricity loss, which is The most important criterion for minimum power is Recent interest in reversible logic in VLSI design has been considerable[6]. It has numerous applications in low-power CMOS and optical devices. Information processing, DNA computing, quantum computing, and nanotechnology are examples of emerging technologies.Due to knowledge loss, irreversible hardwar ecomputation results in energy loss. Reversible logic enables the system to be executed both forwards and backwards.If the input vector can be uniquely recovered from the output vector and the input and output assignments are one-to-one, the circuit is reversible. This indicates that not only can outputs be uniquely determined from inputs, but inputs can also be uniquely recovered from outputs. If computation becomes information-lossless[7], energy dissipation could be reduced or even eliminated.

PERES GATE

On Figure 4, the Peres gate is depicted. [10]The respective vectors for the input, output, and input are A, B, and C (P, Q, R). P = A, Q = A xor B, and R = AB xor C[6][7] decide on the result.The quantum cost of the Peres gate is 4. The Peres gate has the lowest quantum cost in the intended layout. —is utilised. When C is set to 0, Peres' gate functions as a half adder[7]; this module is utilised in full adder[7] and

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ripple carry adder designs. Thus, the need for any external hardware circuitry is eliminated as the same hardware block is used for multiple mathematical operations.

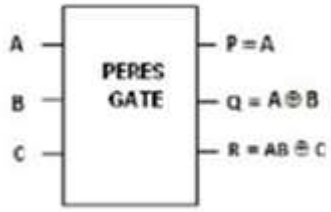

Figure 4 : Peres gate

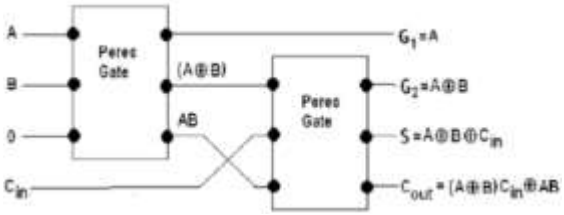

Figure 5: Full adder using reversible logic gates

5.RESULTS

RTL SCHEMATIC:The blueprint for the design is called the RTL, or register transfer level. It is used to evaluate architectural designs to the ideal architecture and assess it.The conversion of the data into the architectural summary into a coded language, such as i.everilog or vhdl. In order to facilitate study, the RTL schematic includes details on the internal connection blocks.The image below depicts the RTL schematic diagram of the planned architecture.

Figure7: RTL Schematic of Proposed vedic multiplier

TECHNOLOGY SCHEMATIC:The VLSI design estimation procedure makes use of the LUT as a parameter of area, and the technology schematic generates an image of the architecture in the LUT format.The code's memory allocation is displayed as a FPGA lookup tables as a square unit.

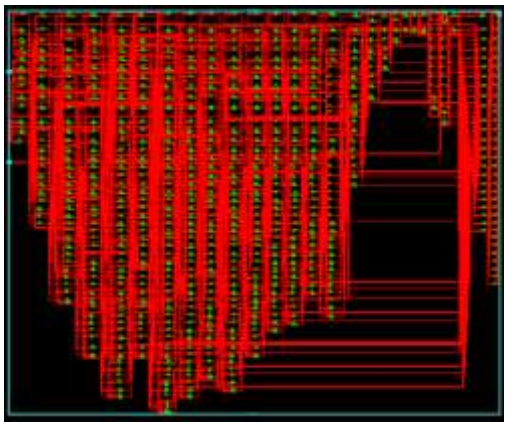

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Figure8:View Technology Schematic of proposed vedic multiplier

SIMULATION:The schematic is used to verify the links and components, while the simulation represents the process. The main screen's simulation window opens when the user switches the tool from implantation mode to simulation mode. The results can only take the shape of waves within the simulation window. As such, it can accommodate a wide range of alternative radix number systems..

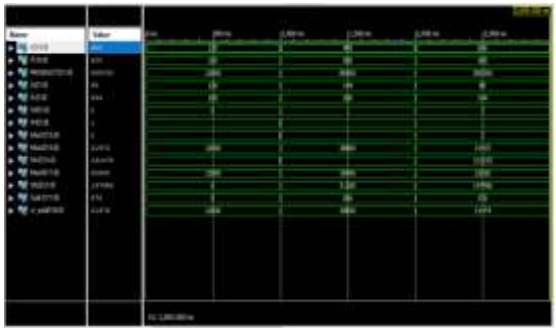

Figure9:Simulated Waveforms of proposed vedic multiplier

PARAMETERS:VLSI metrics such as area, delay, and power can be utilised to evaluate different designs. Here, we address both spatial and energetic dimensions. They are derived from the HDL language and the XILINX 14.7 software. Verilog.

Parameter	Karatsuba Multiplier	Karatsuba Multiplier using Reversible logic
Power (Watt)	2.819	1.661
Number of LUTs	397	234

Table 2: parameter comparison observed in xilinx

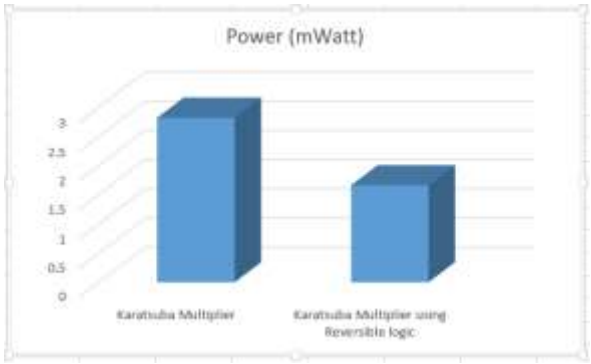

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Figure10: Power comparison bargraph

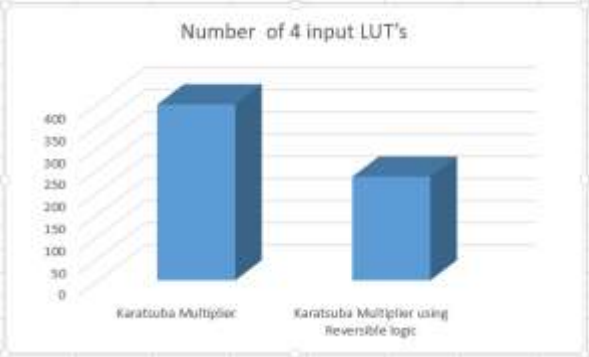

Figure11: LUT comparison bargraph

CONCLUSION

Reversible logic has been proposed and used to demonstrate a 1616-bit multiplier, with the main goal of minimising the latency so that it can be used in DSP, image processing, and computationally intensive ASIPs. Its foundation is the Vedic Karatsuba algorithm, which produces fewer partial product terms. In order to increase speed, the technique is further optimised utilising an adaptive idea for computing the third product term. Additionally, by combining the carry save adders with the suggested Square Root Carry Select Adder (SRCSA) adder with reversible logic as discussed in this article, the compression speed of the partial product terms is also improved. The verilog HDL language is used for the implementation, synthesis, and simulation in the XILINX-ISE tool.The addition of the approximation to the design and the use of this multiplier implementation, which removes gate delays, will improve performance in dsp applications, image processing, filters, and cryptography applications in the future. Applications that are based on area and speed will be used in the future.

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