Design and Optimization of Combinational Circuit using Reversible Logic

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Abstract:

Today's technology world demands high complexity and high-performance system design approach. This technology growth demands high power consumption due to their high complexity and performance. But in the mobile or handheld battery-operated device should consume the low profile energy then only the life span of the device further increased. To address the low power consumption, todays VLSI design adopts the various methods. Apart from, one of the upcoming and new technology is called a reversible logic design, which dissipates less energy. To get low power consumption and decrease in delay, the combinational circuits are implemented by using reversible logic. Reversible logic supports the process of running the system both forward and backward. The reversible gate has the same number of input and output terminals. Reversible logic has the advantages of reducing gate counts, garbage outputs as well as constant inputs. Addition, subtraction operations are realized using a reversible gate and compared with conventional gates. The proposed reversible logic gate is used to design of reversible 4-bit parallel adder circuit and realization of different logic functions such as NOT, AND, NAND, OR, NOR, XOR, XNOR. There are many reversible logic gates has been used by such as MZI, Toffoli gate, Feynman gate, HNG, TSG etc. By using these logic gates, we can implement the combinational circuits to reduce the power dissipation and area optimized. The design has been written in VHDL and simulated by Xilinx 14.1 design software. The synthesized design has been implemented by using Spartan 3E and power has been calculated & compared it.

Key words: Reversible logic, low power reversible logic, combinational design, area, delay, garbage output.

I.INTRODUCTION

Low power design has emerged as a principal theme in today's world of electronics industries. The major concern for VLSI designers is an area, power consumption and delay. Power dissipation has become an important parameter for VLSI design. The low power design is introduced in portable systems. Because it needs less weight, cooling cost and size. In low power design, there are so many abstract levels have been used to achieve it. The low power high-performance digital VLSI design methodologies are being used in circuit's level, gate level, architectural and algorithm level design[11].

The increasing prominence of portable systems and the need to limit power consumption and hence, heat dissipation in very-high density chips have led to rapid and innovative developments in low-power design during the recent years. The driving forces behind these developments are portable applications requiring low power dissipation and high throughput. The need for low-power design is also becoming a major issue in high-performance digital systems, such as microprocessors, digital signal processors (DSPs) and other applications.

Power dissipation is one of the most important factors in VLSI circuit design. Due to the information loss in irreversible hardware computation, it results in energy dissipation. Part of the energy dissipation is due to the non-identity of switches. Because of the higher level of integration and use of a new fabrication process have dramatically reduced the heat loss over the last decades. Todays handheld design uses the low power design because of changing trends in the design, packaging and cooling cost dramatically increase in high density packing devices. Until recently, performance of a processor has been synonymous with circuit speed or processing power, million instruments per second (MIPS) or million floating point operations per second (MFLOPS). Power consumption was of secondary concern in designing of IC's. However, in nanometer technology, power has become the most important issue because of increasing transistor count, Higher speed of operation and greater device leakage currents

Increased process parameter variability due to aggressive device size scaling has created problems in yield, reliability and testing. As a consequence, there is a change in the trend of specifying the performance of a processor. Power consumption is now considered one of the most important design parameters. Among various reasons for this change in trend, some important reasons are considered below. To continuously improve the performance of the circuits and to integrate more and more functionality in the chip, the device feature size has to continuously shrink. There is an escalation in the cost of packing and cooling has the power dissipation increases. To make a chip commercially it is necessary to reduce the cost of packing and cooling, which in turn demands lower power consumption.

This paper is organized as follows: Section 2 describes the Literature survey. Section 3 reversible logic design . Section 4 Result and discussion. Section 5 gives the conclusion.

2. LITERATURE SURVEY

In this section, detailed literature review is done that aims to review the critical points of current works. Here the information collected about researches and innovations carried out on the related technologies have been done. This section will highlight the recent trends and innovations in the concerned technology.

Gordon. E. Moore [1] in 1965 predicted that the numbers of components on the chip will double every 18 months. As the number of components in the chip increases the power dissipation will also increase tremendously. Hence power minimization has become an important factor for today's VLSI engineers. In 1961, R.LANDAUER [2] described that the logical irreversibility is associated with physical irreversibility and requires a minimal heat generation per machine cycle. For irreversible logic computations, each bit of information lost generates kTlog2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In conventional system the millions of gates used to perform logical operations. Author proved that heat dissipation avoidable if system made reversible.

C.H.Bennett [3] stated that this heat dissipation problem can be solved by using reversible computation. Reversible computing follows the property of reversibility in which there is one to one mapping between the input and output vectors. A circuit is set to be reversible if the input vectors can be retrieved from the output vectors. In this research, different papers in which proposed designs are compared with the previous designs. The proposed designs make use of different reversible gates such as Feynman Gate, Fredkin Gate, Toffoli Gate, HNG and TSG Gate etc.., These reversible logic gates makes them better than the previous designs in terms of quantum cost, number of garbage outputs, constant inputs and power consumption. These designs can be used in quantum computing and nanotechnology. He described that if a computation is carried out in Reversible logic zero energy dissipation is possible, as the amount of energy dissipated in a system is directly related to the number of bits erased during computation. The design that does not result in information loss is irreversible. A set of reversible gates are needed to design reversible circuit. Reversible gate can generate unique output vector from each input vector and vice versa.

Soolmaz Abbasalizadeh [4] has designed 4-Bit Comparator Based on Reversible Logic Gates. Here he explained that reversible logic has been considered as one of the promising practical strategies for power-efficient computing. In fact, when the inputs can't be recovered from circuit's outputs, information loss appears. Reversible logic circuits can handle this issue. In this logic, one to one mapping exists between the inputs and outputs. The number of inputs and outputs are equal, and inputs can be recovered from outputs. The parameters such as number of reversible gates, number of constant inputs, garbage outputs and quantum cost can be named as optimization parameters.

Edward Fredkin and Tommaso Toffoli [5] introduced new reversible gates known as fredkin and Toffoli reversible gates based on the concept of reversibility. These gates have zero power dissipation and are used as universal gates in the reversible circuits. These gates have three outputs and three inputs, hence they are known as 3*3 reversible gates. Also introduced based on the concept of reversibility they introduced a new reversible gate known as Fredkin and Toffoli reversible gates. These gates have zero power dissipation and are used as universal gates in the reversible circuits. These gates have three input and three outputs; hence they are known as 3*3 reversible gates. In the year 1994 Shor [6] did a remarkable research work in creating an algorithm using reversibility for factorizing large number with better efficiency when compared to the classical computing theory. After

this the work on reversible computing has been started by more people in different fields such as nanotechnology, quantum computers and CMOS VLSI.

Peres [7] introduced a new gate known as Peres gate. Peres gate is also a 3*3 gate but it is not a universal gate like the Fredkin and Toffoli gate. Even though this gate is not universal gate it is widely used in many applications because it has less quantum cost when compared universal gate. The quantum cost of the Peres gate is 4. H Thalpliyal and N Ranganathan [8] invented a reversible gate known as TR gate. The main purpose of introducing this reversible TR gate was to decrease the garbage output in a reversible circuit. H Thalpliyal and N Ranganathan [9] introduced the reversible logic to sequential circuits. Implementation of the sequential circuit such as D-latch, T latch, JK latch and SR latch using Fredkin and Feynman gate has been done. After this work more research has been done on sequential circuits using reversible gates. Using the combination of Fredkin and Feynman gate a new gate known as Sayem gate was proposed by Sujata S. Chiwande Prashanth R. Yelekar [10] sayem gate is a 4*4 reversible gate and is used in designing sequential reversible circuits.

M.L. Chuang and C.Y. Wang [11] proposed that the numbers of gates, the number of garbage output were reduced in implementing the Latches and when the results will be compared [10] with 25% improvement was achieved. Based on the above research and work done, they are going to implement the reversible logic concept for sequential circuits such as D-flip flop, T-flip flop and the 4-bit asynchronous counters. Arunkumar P Chavan [12] has proposed the pulse detector and unsigned multiplier. He also explained the 4-Bit reversible PISO Shift register. Here the 4-bit PISO shift registers uses four reversible clocked D flip-flops and four Fredkin Gates. Reversible Fredkin Gate is used to develop a multiplier with an enable signal. Similarly a basic 3-bit reversible SIPO shift register can be constructed using three reversible clocked D flip flops and two Feynman gates.

Gopal, Lenin; Mohd Mahayadin and Nor Syahira [13] investigated the ALU designed to show its major implications on the Central Processing Unit (CPU).In this paper, two types of reversible ALU designs are proposed and verified using Altera Quartus II software. In the proposed designs, eight arithmetic and four logical operations are performed. In the proposed design 1, Peres Full Adder Gate (PFAG) is used in reversible ALU design and HNG gate is used as an adder logic circuit in the proposed ALU design 2. Both proposed designs are analysed and compared in terms of number of gates count, garbage output, quantum cost and propagation delay. The simulation results show that the proposed reversible ALU design 2 outperforms the proposed reversible ALU design 1 and conventional ALU design. Kaur, T. and Singh, N. [14], In this research work, the basic concepts of reversible circuits are briefly discussed. Furthermore, an efficient & low cost fault tolerant reversible Arithmetic and logical unit (ALU) is designed and implemented. The results are then compared with the existing design. The large garbage outputs in the proposed design are compensated by the number of operations that it can perform. The Proposed design can perform almost all arithmetic and logical operations on the other hand existing design performs only four operations.

Rakshith, T.R. and Saligram, R. [15] estimated the power dissipation is an important design criterion during the VLSI process flow. Reversible logic is one of the promising fields having a wide range of applications starting from low power VLSI design, fault tolerant circuits, quantum computing to fields such as bio informatics. An ALU may be regarded as the processor's numerical calculator and logical operation evaluator. In this paper a fault tolerant reversible ALU design is proposed. Parity preserving logic gates are the main component in this design. A parity preserving gate is the one in which the parity of the input and the output vectors is the same. The proposed ALU can produce up to 16 logical and 16 arithmetic operations.

Syamala, Y. and Tilak, A.V.N., [16] researched on a function is reversible if each input vector produces a unique output vector. Reversible logic is of growing importance to many future computer technologies. In this paper, the design of a reversible Arithmetic Logic Unit (ALU) is presented making use of multiplexer unit as well as control signals. ALU is one of the most important components of CPU that can be part of a programmable reversible computing device such as a quantum computer. In multiplexer based ALU the operations are performed depending on the selection line. The control unit based ALU is developed with 9n elementary reversible gates for four basic arithmetic logical operations on two n-bit operands. The series of operations are performed on the same line depending on control signals, instead of selecting the desired result by a multiplexer. The later design is found to be advantageous over the former in terms of number of garbage outputs and constant inputs produced.

In 2014, Neeta Pandey et.al,proposed 2:4 reversible decoder and 3:8 reversible decoder using Feynman and Fredkin gate. They also implemented Feynman and Fredkin gate using transmission gates. They were also compared the various parameters of proposed decoders with exiting decoders [17]. In july 2014, Ashima Malhotra, et.al, proposed different types of reversible multiplexers using modified Fredkin gate. They were proposed 2:1, 4:1, 8:1 and 16:1 reversible multiplexers. They were also compared with quantum cost and power consumption of proposed reversible multiplexers with exiting one [18]. In July 2014, Ashima Malhotra, et.al, described that reversible modified Fredkin gate used to designed multiplexers. They also compared the quantum cost of multiplexers designed using Fredkin gate with multiplexers designed using modified Fredkin gate[19]. Panchal et al.[20] (2013) proposed an 4x4 reversible multiplier circuit which is implemented using Peres and Toffoli reversible gate and compared with the existing designs , The proposed reversible multiplier is better in terms of hardware complexity, number of gates, garbage output, constant inputs and total quantum cost.

H.Thapliyal, M .B. Srinivas and Mark Zwolinski [21] proposed a reversible D -flip-flop using New gate and Feynman gate. The drawback of this work is that it requires more number of reversible gates and produces more number of garage outputs. As the number of reversible gates required is more, it also increases the quantum cost of their flip-flop. H.Thapliyal and M.B.Srinivas [22] proposed a reversible D-latch using two Fredkin gates. The drawback of their work is the quantum cost to realize a reversible D-latch with both the outputs Q and Q' is 10. However, to realize a reversible master-slave D-flip-flop 5 Fredkin gates are used which increases t he quantum cost. Rice [23] proposed a reversible S R latch and all the other latches were designed as the sub-units from reversible RS latch as a part of master-slave flipflops.

Thapliyal and Vinod [24] proposed the designs of reversible latches and flip flops. The proposed designs were shown to be better than the designs presented in Rice [23] in terms of the number of reversible gates and garbage outputs. The quantum cost of the reversible D-latch proposed by Thapliyal and Vinod is 10. H.Thapliyal and N.Ranganathan [25] proposed a negative enabled reversible D - Latch using Fredkin gate. The advantage of this work is that it does not require the inversion of CLK pulse to realize the master-slave D-flip-flop. To realize both the outputs Q and Q', it requires 1 Fredkin gate and 2 Feynman gates and the quantum cost of their implementation is 7. The transistor implementation is not addressed in this work. Md. Selim Almamun, Indrani mandal, Md. Hasanuzzaman [26] proposed a reversible D-latch using MG-1 gate. In this work the number of XOR operations involved in realizing a M G-1 gate is more which will increase the transistor count.

S.Ranjith, T.Ravi and E.Logashanmugam [27] proposed a reversible R R gate using which a reversible D-Flip-flop has been realized. The drawback of their work is that to realize a master slave flip-flop an additional reversible gate is required to produce the complement of the clock signal and further to realize the flip-flop with both the outputs Q and Q' one more reversible gate is in need to produce Q'. Thus, the number of reversible gates required is more which in addition will increase the transistor count.

3. PROPOSED WORK

Reversible logic:

Reversible are circuit (gates) in which one to one mapping between inputs and outputs. Reversible logic supports the process of running the systems both forward and backward. The amount of energy dissipation in a system increases in direct proportion to the number of bits that are erased during computation. Bennett showed that KTln2 energy dissipation would not occur, if a computation is performed in a reversible way. Reversible computation in a system can be performed if the system is composed of reversible gates. The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit [4]. The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Minimum number of gates is used for implementation

- Restrict the number of garbage outputs as fewer as possible.
- Design should cater all the good features of reversible logic synthesis.

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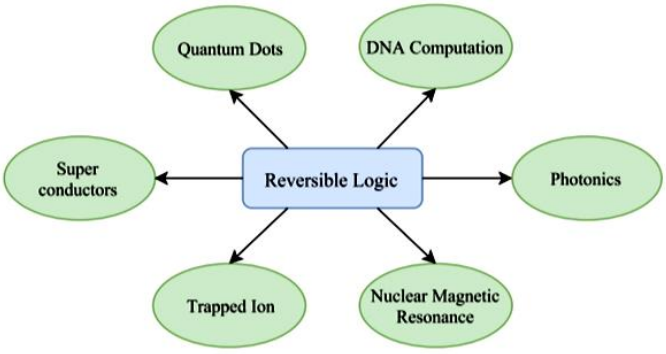

Figure 1: Different Forms of Reversible Logic

In the reversible logic, to prevent the loss of bit in logical operation, the number of inputs & outputs are made equal. Reversible gate is an n*n gate in which outputs can regenerate inputs, where n is number of inputs or outputs as shown in Fig2. To minimize the power dissipation, reversible logic gates are used instead of irreversible logic gates. In reversible gates, inputs & outputs are mapped one to one which will conserve energy as there will not be a loss of any bit.

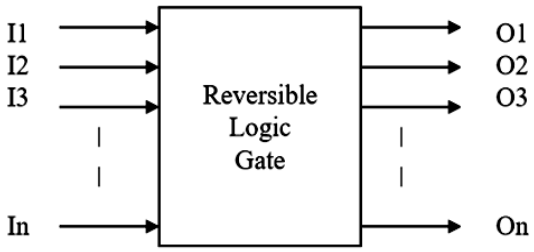

Figure 2: Block Diagram of Reversible Logic Gate

Features of reversible logic circuit:

I. Minimum number of reversible gates is used.
II. Minimum number of constant inputs is used.
III. Minimum number of garbage outputs should be there.
IV. The cascading gates length is minimum.

Fundamental properties of Reversible logic:

Garbage Output:
To maintain the bijectivity property in the realization of reversible circuits, some outputs are left unused. These outputs are referred as Garbage Outputs (GO).
Ancilla Input:
There are the requirements of additional constant inputs to convert an irreversible into reversible circuit. These additional inputs are referred as Ancilla Input.
Power Consumption:
The CMOS implementation using four transistor logic comprises of the reduced power consumption. A large part of the power consumption is caused by the frequent switching of inverters, the once that are connected to the input ports. The short circuit current is established by a direct path between VDD and VSS. The repeated presence of such connection causes higher power consumption. This part of the power is less when direct paths from VDD to VSS are limited or became nonexistent when either VDD or VSS is not present. The implemented designs in this research work have this advantage and thus they offer low power consumption.
Design utilization: Number of LUTs, number of gates and number of occupied slices
Device utilization is another objective for the low power VLSI Design. The implementation using Xilinx ISE shows that the combinational circuits, sequential circuits and low pass FIR Filters designed

using proposed gate are efficient in terms of LUTs used, number of occupied slices and number of gates used.

Quantum Cost:

A complete reversible circuit can also be realized in corresponding quantum realization using elementary quantum gates. The sum of these elementary quantum gates are termed as Quantum Cost (QC) of the circuit.

Goals of reversible logic gate:

- Minimize the garbage
- Minimize the width of the circuit
- Minimize the total number of gates
- Minimize the delay

Basic reversible logic gates:

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. A reversible logic gate is a memory-less logic element that realizes an injective logical function. It has the advantages of reducing the power consumption, decrease in delay, reducing the number of counts and reduces the area.

- Not Gate
- Feynman Gate
- Toffoli Gate
- Fredkin Gate
- Peres Gate
- HN(Haghparast - Navi) Gate
- TS(Test Set) Gate

Combinational Circuit:

Combinational logic circuits are memory less digital logic circuits whose output at any instant in time depends only on the combination of its inputs. These are made up of different types of logic gates.**Ex:** Encoder, Decoder, Multiplexer, Comparator, Adder, 4-bit Parallel adder.

Combinational circuit using Reversible logic:

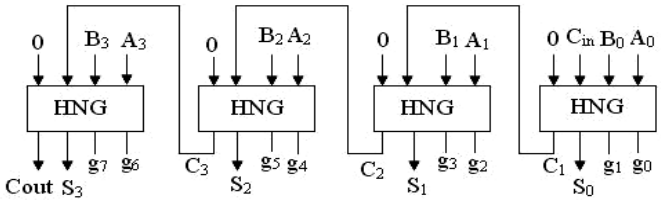

Figure 3: Reversible 4-bit parallel adder

Figure 3 shows an optimized reversible 4-bit parallel adder using a HNG reversible gate.

4.RESULTS AND DISCUSSION

The following demonstrates that the proposed reversible 4-bit parallel adder gate is superior to the existing counterparts in terms of hardware complexity, power, area, delay, garbage outputs and constant inputs. The simulated output waveforms for reversible 4-bit parallel adder using HNG and TSG gates are shown in Fig4 and Fig5.

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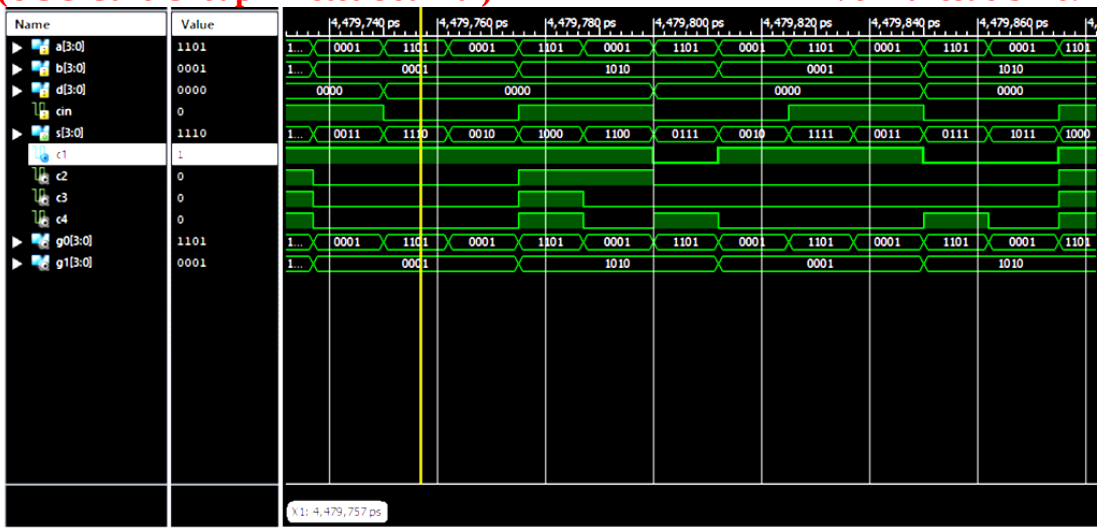

Figure 4: Simulated Output for Reversible 4-bit Parallel Adder using HNG Gate

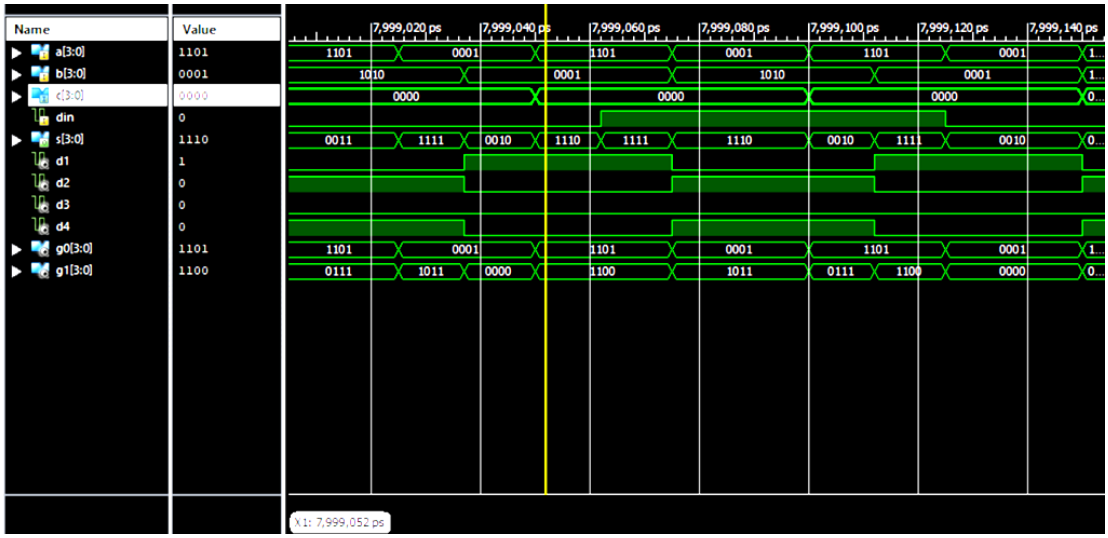

Figure 5: Simulated Output for Reversible 4-bit Parallel Adder using TSG Gate

Design summary of reversible 4-bit parallel adder using HNG gate and TSG gate is shown in Fig7 and Fig8. It shows the usage of number of input LUT's, number of occupied slices and IOB properties.

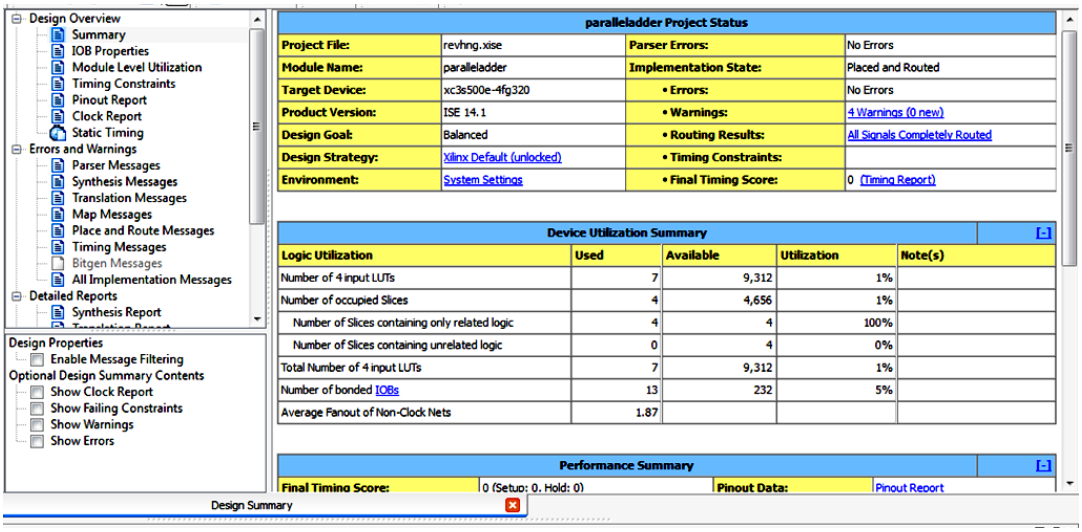

Figure 6: Design Summary of Reversible 4-bit Parallel Adder using HNG Gate

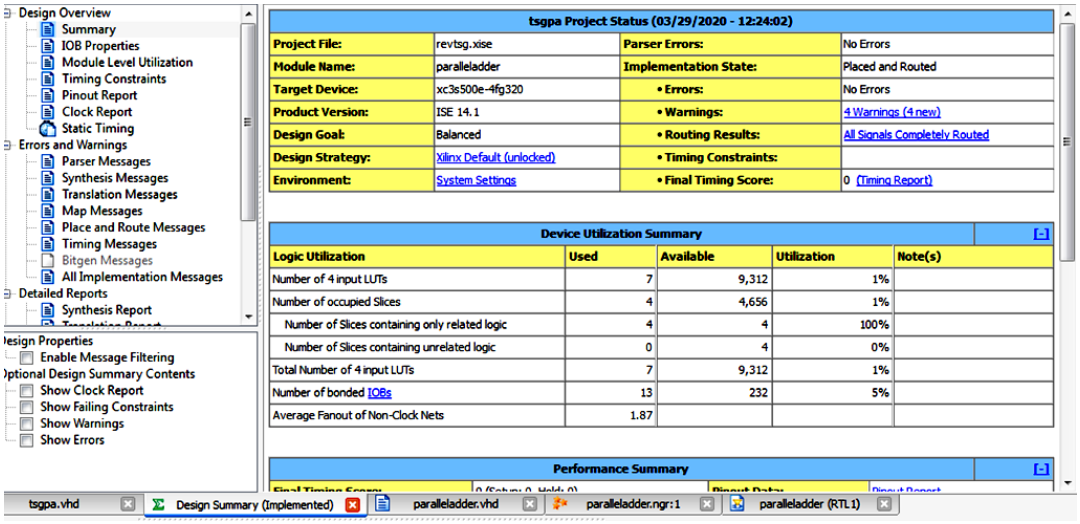

Figure 7: Design Summary of Reversible 4-bit Parallel Adder using HNG Gate

5 CONCLUSION

In this paper, a 4-bit parallel adder combinational circuit constructed using reversible HNG and TSG logic gate is implemented using FPGA. Implementation of combinational circuit using reversible logic is to reduce the power dissipation, area optimization, delay, complexity and garbage outputs.

REFERENCES

1. Gordon. E. Moore, "Cramming more components onto integrated circuit", *Electronics*, pp. 114-117, 1965.
2. Landauer. R, "Irreversibility and heat generation in the computing process", IBM J. Research and Development, pp.183-191, 1961.
3. Bennett C.H., "Logical reversibility of Commutation". IBM Research and Development, pp. 525-532, 1973.
4. Soolmaz Abbasalizadeh., "4-Bit Comparator Deign Based on Reversible Logic Gates". IEEE transaction 2013.
5. E. Fredkin, T Toffoli, "Conservative Logic", International Journal of Theory Physics, pp. 219-253, 1982.
6. P. Shor, "Algorithms for quantum computation: discrete log and factoring", IEEE Computer Society, Los Alamitos, pp. 124 -34, 1994.
7. A. Peres, "Reversible Logic and Quantum Computers", Physical Review, pp. 3266-3276, 1985.
8. H Thapliyal and N Ranganathan, "Design of Efficient Reversible Binary Subtractors Based on a New Reversible Gate", IEEE Proceedings of the Computer Society Annual Symposium on VLSI, pp. 229-234, 2009.
9. H Thapliyal and N Ranganathan, "Design of Reversible Latches Optimized for Quantum Cost, Delay and Garbage Outputs", Proceedings of Twenty Third International Conferences on VLSI Design, pp. 235-240, 2010.
10. Sujata S. Chiwande and Prashanth R. Yelekar, "Design of sequential circuit using reversible logic", IEEE-International Conference Advances in Engineering, Science and Management, pp. 321-326, 2012.
11. M. L. Chuang and C.Y. Wang,"Synthesis of reversible sequential elements", ACM journal of Engineering Technologies in Computing Systems, 420 -425, 2007.
12. Rajasekar, P., and H. Mangalam. "Design and implementation of low power multistage AES S box." *International Journal of Applied engineering Research* 10 (2015): 40535-40540
13. Arunkumar P Chavan., "Design of Pulse Detector and Unsigned Sequential Multiplier using Reversible Logic".International journal on computer application, April 2014.
14. Gopal, Lenin; Mohd Mahayadin, Nor Syahira; Chowdhury, Adib Kabir; Gopalai, Alpha Agape; Singh, Ashutosh Kumar, "Design and synthesis of reversible arithmetic and Logic Unit (ALU)," Computer,

ISSN: 2278-4632
Vol-10 Issue-5 No. 1 May 2020

Communications, and Control Technology (I4CT), 2014 International Conference on , vol., no., pp.289,293, 2-4 Sept. 2014.
15. Kaur, T.; Singh, N., "Design of Fault Tolerant Arithmetic & Logical Unit Using Reversible Logic," Machine Intelligence and Research Advancement (ICMIRA), 2013 International Conference on pp.331,334, 21-23 Dec. 2013.
16. Rakshith, T.R.; Saligram, R., "Parity preserving logic based fault tolerant reversible ALU," Information & Communication Technologies (ICT), 2013 IEEE Conference on pp.485, 490, 11-12 April 2013.
17. Syamala, Y.; Tilak, A.V.N., "Reversible Arithmetic Logic Unit," Electronics Computer Technology (ICECT), 2011 3rd International Conference on pp.207, 211, 8-10 April 2011.
18. Neeta Pandey,Nalin Dadhich, Mohd. Zubair Talha, '' Realization of 2:4 reversible decoder and its applications", International Conference on Signal Processing and Integrated Networks (SPIN).IEEE, 2014.
19. Rajasekar, P. and Mangalam, D. (2016) Efficient FPGA implementation of AES 128 bit for IEEE 802.16e mobile WiMax standards. *Circuits and Systems*, **7**, 371-380. doi: 10.4236/cs.2016.74032
20. Ashima Malhotra, Charanjit Singh, Amandeep Singh, ''Efficient Design of Reversible Multiplexers with Low Quantum Cost and Power Consumption'', International Journal of Emerging Technology and Advanced Engineering, 7, July 2014.
21. Ashima Malhotra, Charanjit Singh, Amandeep Singh,"Efficient Design of Reversible Multiplexers with Low Quantum Cost", Int. Journal of Engineering Research and Applications, July 2014.
22. Vijay K Panchal, Vimal H Nayak, "Analysis of multiplier Circuit using Reversible Logic" , International Journal for Innovative Research in Science & Technology, pp-2349-60, 10,Nov 2013.
23. H.Thapliyal, M.B. Srinivas, M.Zwolinski, "A beginning in the reversible logic synthesis of sequential circuits", Proceedings of the International Conference on the Military and Aerospace Programmable Logic Devices 2005.
24. H.Thapliyal, M. B. Srinivas, An Extension to DNA Based Fredkin Gate Circuits "Design of Reversible Sequential Circuits using Fredkin Gates", SPIE International Symposium on Optome chatronic Technologies Sapporo, Japan, December, 2005.
25. J. Rice, A new look at reversible memory elements, Proceedings of the International Symposium on Circuits and Systems pp. 243– 246, 2006.
26. Rajasekar, P., and H. Mangalam. "Design and implementation of low power multistage AES S box." International Journal of Applied engineering Research 10 (2015): 40535-40540.
27. H. Thapliyal, A. P. Vinod, Design of reversible sequential elements with feasibility of transistor implementation, Proceedings of the IEEE International Symposium on Circuits and Systems pp. 625–628, 2007.
28. H. Thapliyal, N. Ranganathan, "Design of Reversible Sequential Circuits Optimizing Quantum Cost, Delay, and Garbage Outputs", ACM Journal of Emerging Technologies and Computer Systems, 2010.
29. Md. Selim AlMamun, I. Mandal, Md. Hasanuzzaman, Efficient Design of Reversible Sequential Circuit, IOSR Journal of Computer Engineering (IOSRJCE), pp. 4247, 2012.
30. S. Ranjith, T. Ravi, E. Logashanmugam, "Design and Analysis of Parity Preserving Fault Tolerant Reversible Logic Shift Registers Using New 4*4 R R-Gate", International Journal of Advanced Research in Computer Science and Electronics Engineering (IJARCSEE), pp. 165-171, 2013.