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DESIGN OF 8 BIT VEDIC MULTIPLIER USING GDI TECHNIQUE

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ABSTRACT

Multiplier is the common hardware block present in any processor.Speed and power consumption become very vital in multiplier design consideration to conserve energy. A 8 bit Vedic multiplier using GDI technique is designed in this paper. Multiplication of two numbers will take more time and many steps. To design the proposed multiplier the Vedic mathematics sutra called UT is used. Any logic circuit can be designed by using CMOS logic. The CMOS logic will consumes more area. The numbers of transistors in the circuit are reduced by using GDI logic. Thus the Vedic mathematics will reduce the delay and the GDI logic will reduce the transistors count in a circuit which in turn reduces the power.

Keywords: GDI technique, Vedic mathematics.

1. Introduction

Multiplication is the most important arithmetic operation in signal processing applications. All the signal and data processing operations involve multiplication. As speed is always a constraint in the multiplication operation, increase in speed can be achieved by reducing the number of steps in the computation process. The speed of multiplier determines the efficiency of such a system. In any system design, the three main constraints which determine the performance of the system are speed, area and power requirement. Vedic mathematics[1] was reconstructed from the ancient Indian scriptures (Vedas) by Swami Bharati Krishna Tirthaji Maharaja (1884-1960) after his eight years of research on Vedas. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as sutras. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing. Integrating multiplication with Vedic Mathematics techniques would result in the saving of computational time. To design any circuit using CMOS logic we need more number of transistors. As the number of transistors increases the

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power also increases and also area increases. By using GDI technique transistor count is reduced, which in turn reduces the power.

A 8 bit multiplier is designed by using 4 bit multiplier and ripple carry adders. In this paper an efficient use of Vedic Multiplication and GDI techniques are used for the design of 8 bit multiplier has presented.

2. Vedic mathematics:

In ancient times the Indian Mathematics is names as Vedic Mathematics. The Vedic mathematics was again finding from the Vedas by Sri Bharati KrsnaTirthaji (1884-1960) between 1911 and 1918. According to all his research, there are sixteen Sutras in Vedic mathematics.According to him the Coherence is the prominent characteristic of the Vedic mathematics and it is easily understandable. Thus, mathematics is made easy, enjoyable and it motivates for new ideas. Therefore, by using Vedic methods the huge sums or 'difficult' problems are easily solved. Vedic Mathematics[2] is applied in fast calculations like multiplication, division, squaring, cubing and some other. A highly efficient approach is provided by Vedic Mathematics to cover a more range from elementary multiplication to relatively advanced topics.

2.1. “Urdhva-tiryakbyham” Sutra

For any multiplication types “Urdhva-tiryakbyham” Sutra is applicable to all. Using line diagram multiplication of two 2 digit numbers and two 4 digit numbers is shown in Fig.1(a) and fig.1(b) respectively. In Urdhva Tiryakbyham method the numbers from two sides of the lines are taken and multiplied and obtained carry from before step is added. In the first step the resultant bit and a carry is produced. In second step the obtained carry will be added and the process repeats. After that all the obtained results are summed to the preceding carry, when more than one line is there in one step. Result bit is the least significant bit obtained in each step and remaining bits are given as carry for the second step. In the beginning we need to take carry as zero.

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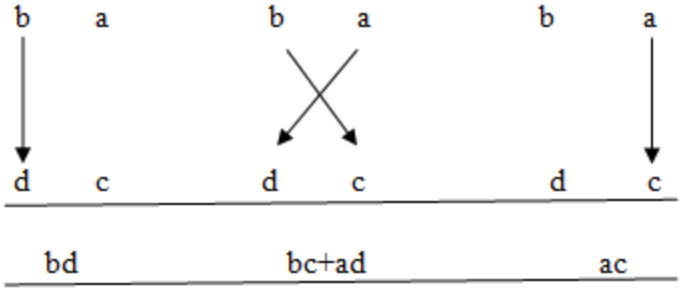

Fig: 1(a) 2*2 Vedic multiplication

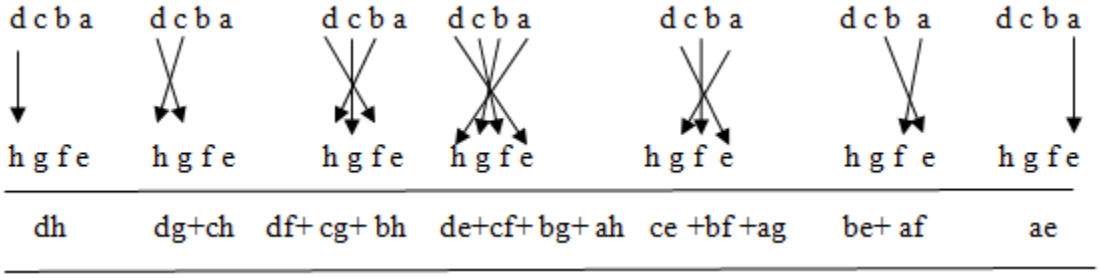

Fig: 1(b) 4*4 Vedic multiplication

3. GDI logic:

In 2002 Morgenshtein[6] et al. invented the GDI logic. Figure 2 shows that the fundamental GDI cell comprises of two transistors. G, P and N are the three inputs of GDI cell. The output is taken from the drain terminals of both the transistors, and one of the input is taken from source terminal of p- type (pMOS) and the other input from is taken from source of a metal oxide semiconductor of n-type (nMOS). The nMOS bulk is connected to ground and the pMOS bulk is connected to supply voltage. Different functions implemented by using GDI logic are shown in table 1. GDI logic has a drawback that is the signal swing is reduced at the output. These signal levels can be restored by using buffers. Table 2 compares the logic circuits transistors count which is implemented by applying GDI (without buffer) logic and CMOS technique. Hence, by using GDI[7] logic any circuit will require fewer number of transistors when compared with other logics.

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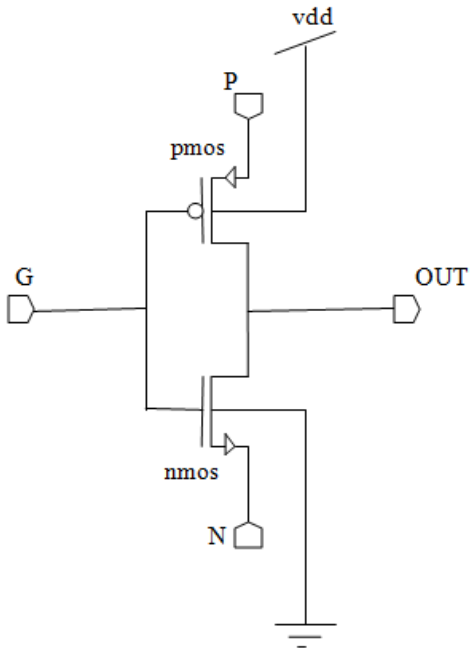

Fig:2 GDI cell

Table1: Different functions implemented using GDI technique

N	P	G	OUTPUT	LOGIC CIRCUIT
0	1	A	A'	NOT
B	0	A	AB	AND
1	B	A	A+B	OR
C	B	A	A'B+AC	MULTIPLEXER

Table 2: logic circuits TC in CMOS and GDI

Logic Circuit	GDI	CMOS
AND	2	6

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XOR	4	12
Half adder	6	18
Full adder	10	28

The schematic output of XOR gate using GDI technique is shown in below figure. This GDI based XOR gate consists of only 4 transistors. Whereas the XOR gate designed by using CMOS logic will contains 12 transistors. The TC (transistor count) is less in GDI logic when compared to CMOS logic.

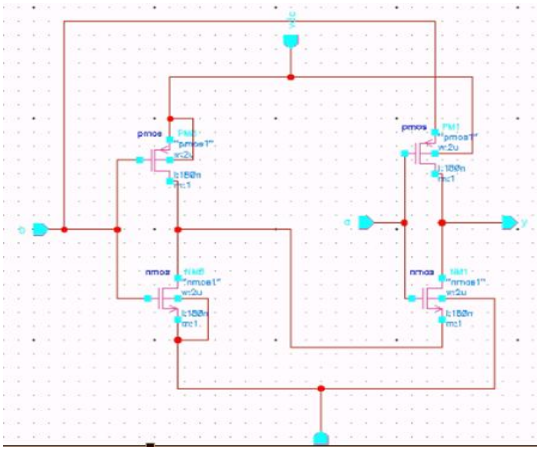

Fig:3 schematic output of GDI- XOR gate

Both the Vedic multiplication and GDI concepts are independently effectual. The delay in the circuit can be reduced by using Vedic multiplication technique and the transistor counts reduced by using GDI logic. As the TC is less dynamic power will be reduced. Hence, gate diffusion input based Vedic multiplier can be effectual.

4. Proposed Multiplier design:

The proposed 8 bit multiplier is implemented using Vedic mathematics based on Urdhva Tiryakbhyam sutra and GDI technique. The proposed multiplier is having 4*4 Vedic multiplier using GDI technique is used as a base block. By using this base block a 8 bit Vedic multiplier[4] using GDI technique is designed.

a. 4 bit Vedic multiplier

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Architecture of 4 bit VM[3] module is shown in fig5. Half adder and full adder blocks are present in the multiplier. In this paper these adders are designed using GDI logic. In 4X4 multiplication, consider the inputs as A and B which are of 4 bits each. Multiplier output will be of 8 bits as – S0 to S7.

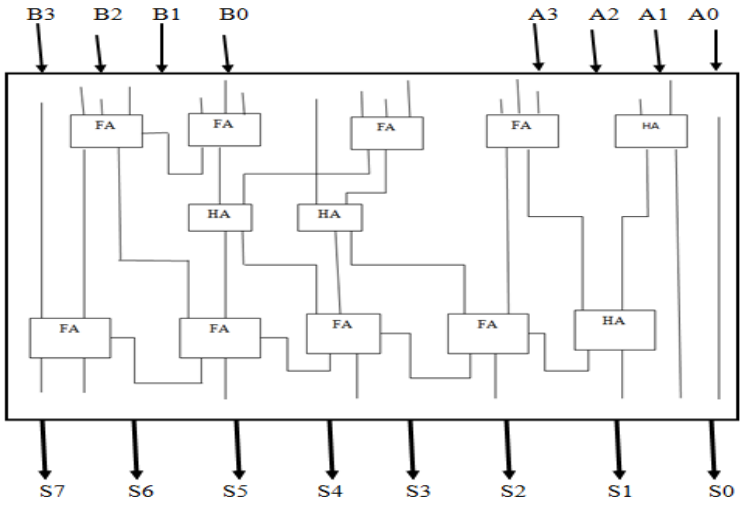

Fig:4 Architecture of 4 bit Vedic multiplier

GDI based full adder design:

In any ALU full adder is a fundamental block which is a nucleus to perform various operations like multiplication, subtraction, division, and address computation as well as additions. Full adders are encountered in the critical path of the complex arithmetic computation like multiplication.GDI based full adder[8] which operates on low power. The circuit level design of GDI based full adder with buffers is shown in figure 5.

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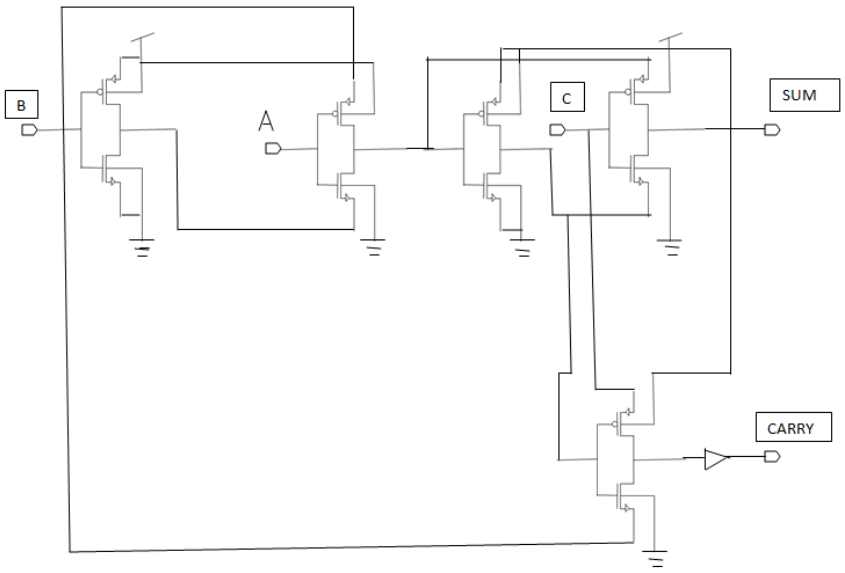

Fig:5 GDI full adder

The schematic output of GDI based full adder is shown in the figure which consists of p-type and n-type MOS transistors. A B and C are given as inputs and outputs are taken as sum and carry.

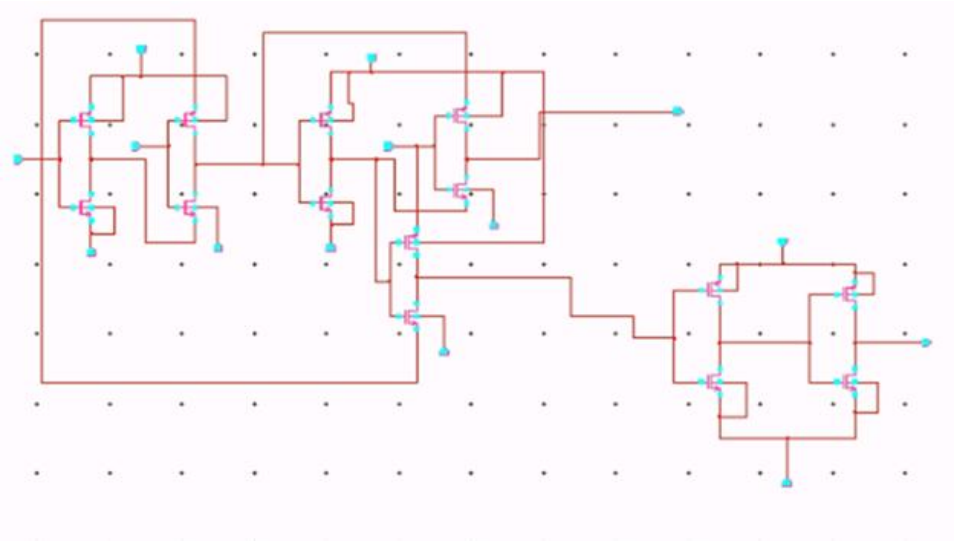

Fig:6 schematic output of GDI based full adder

The 4*4 Vedic multiplier schematic is shown in the below figure. Input from a0 to a4 and b0 to b4 are given. These are given by using AND gate which is designed by using GDI technique. The outputs from the gates are given to the respective full adders and half adders. The corresponding outputs from s0 to s7 are taken.

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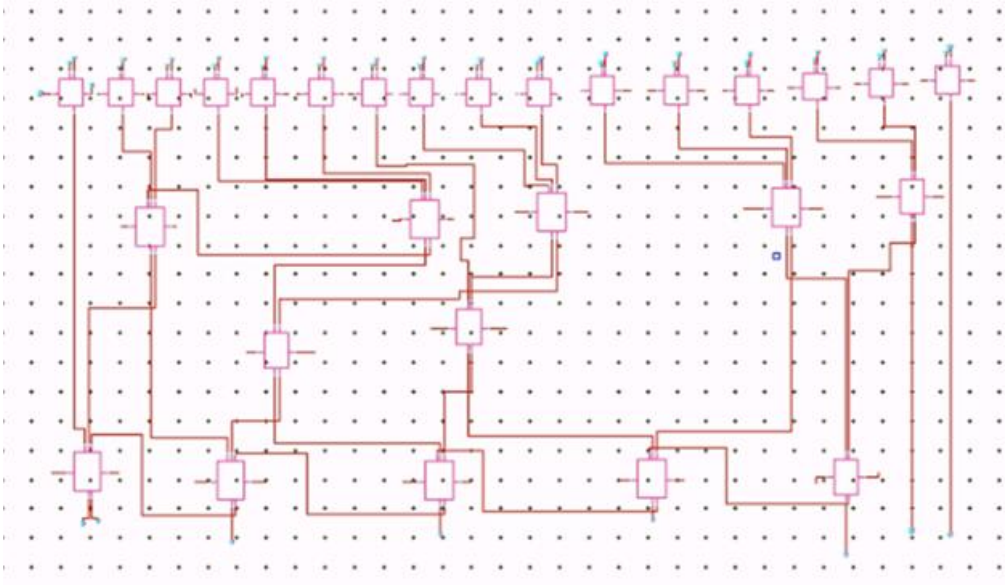

Fig:7 4*4 Vedic multiplier schematic

b. 8 bit vedic multiplier design:

The architecture of 8*8 VM is shown in Fig.8.The 8 bit multiplier[5] design contains four 4*4 Vedic multiplier modules. Let's consider 8x8 multiplications, say the inputs A ranges from a0 to a7 and B ranges b0 to b7. The multiplier output will be of 16 bits as – s0 to s15.Consider an 8 bit multiplicand, in that A can be split into pair of 4 bits that is higher and lower bits (AH-AL). In the same way multiplicand B can be split into BH-BL. The outputs from 4x4 multipliers are given to the ripple carry adders and the addition is performed accordingly to get the final product. In this design three 8 bit Ripple-Carry Adders are needed as shown in Fig.8.The adders are the combination of full adders which are designed used GDI logic. The required outputs from the adders are taken as the 8 bit multiplier product outputs.

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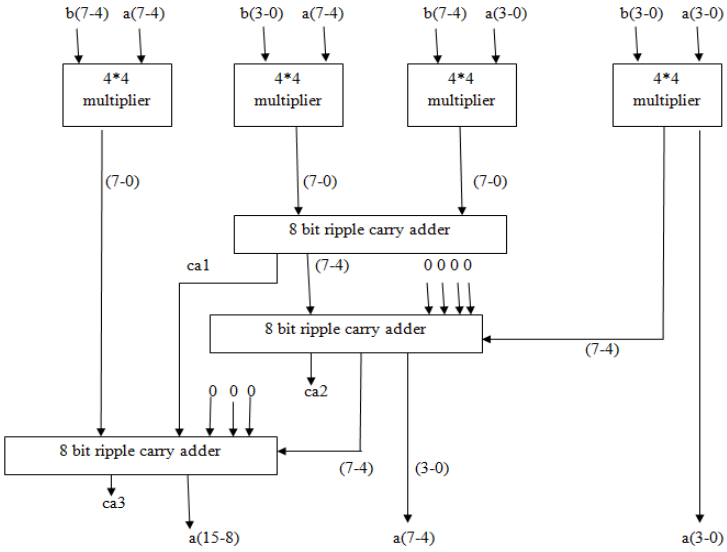

Fig:8 Design of 8 bit Vedic multiplier

Schematic output of 8*8 multiplier design is given in the figure below. The multiplier design will have four 4-bit Vedic multipliers and three adders each of 8 bit. The inputs from a(0-7) and b(0-7) are given and corresponding outputs from s0 to s15 are taken.

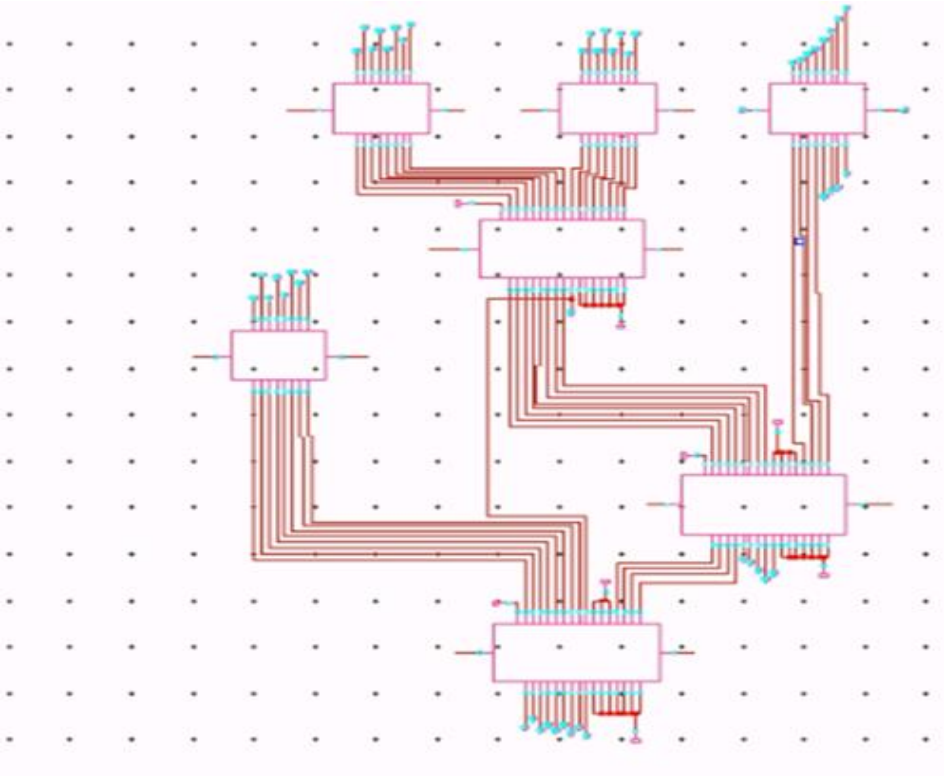

Fig:9 schematic of 8*8 multiplier

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5. Results:

The output wave form for GDI based XOR gate is shown in figure below. There are only 4 transistors required for a circuit to perform XOR operation using GDI logic. Also the output waveforms for the full adder and the proposed multiplier design are shown in below figures. The parameters like power, delay and transistor count are compared for the proposed multiplier and the conventional multiplier is shown in the table below.

Table: 3 comparisons of different designs using CMOS and GDI

Circuit	Power(nW)		Delay (ns)		TC	
	CMOS technique	GDI technique	CMOS technique	GDI technique	CMOS technique	GDI technique
AND	3582	2612	1.56	0.73	6	2
XOR	9530	3512	1.05	0.610	12	4
FULL ADDER	34427	1650	44.2	22.5	28	12
8 BIT VEDIC MULTIPLIER	8299	4428	12.6	5.3	1236	736

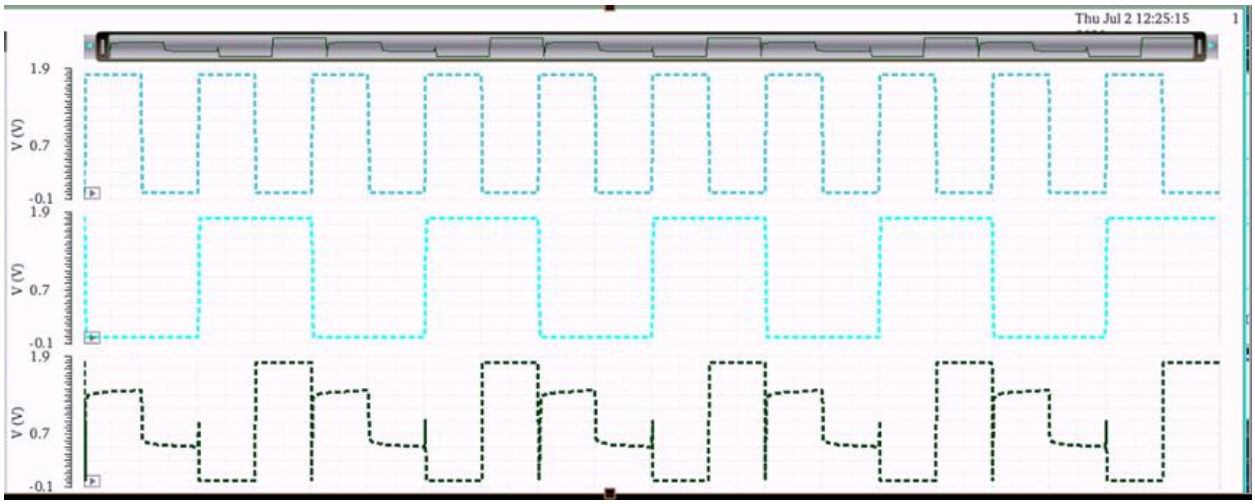

Fig: 10 GDI - XOR gate output

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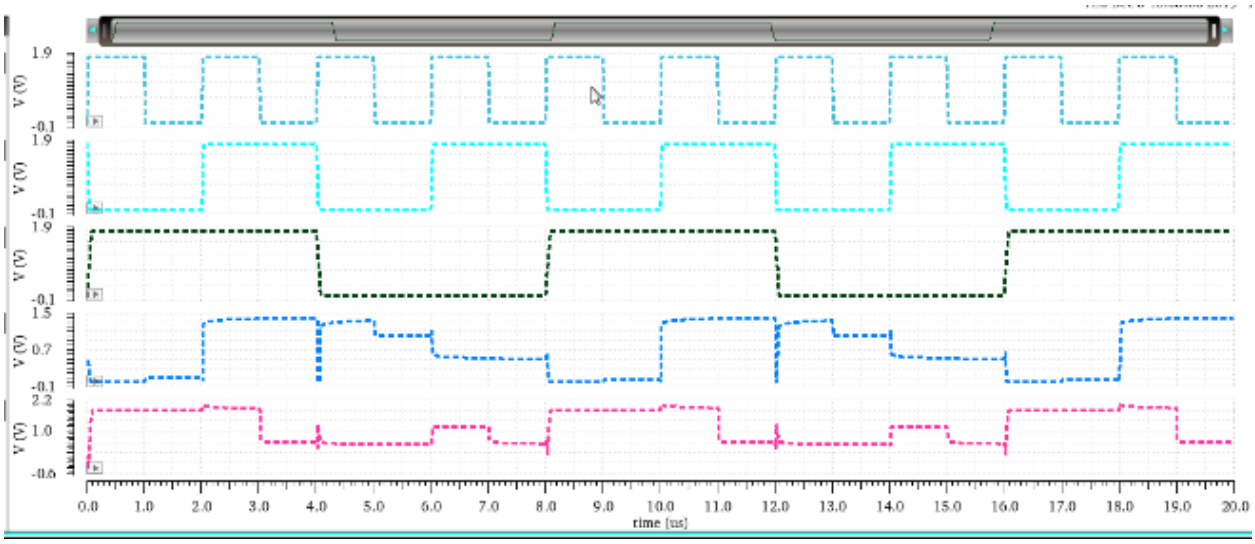

Fig:11 GDI full adder output

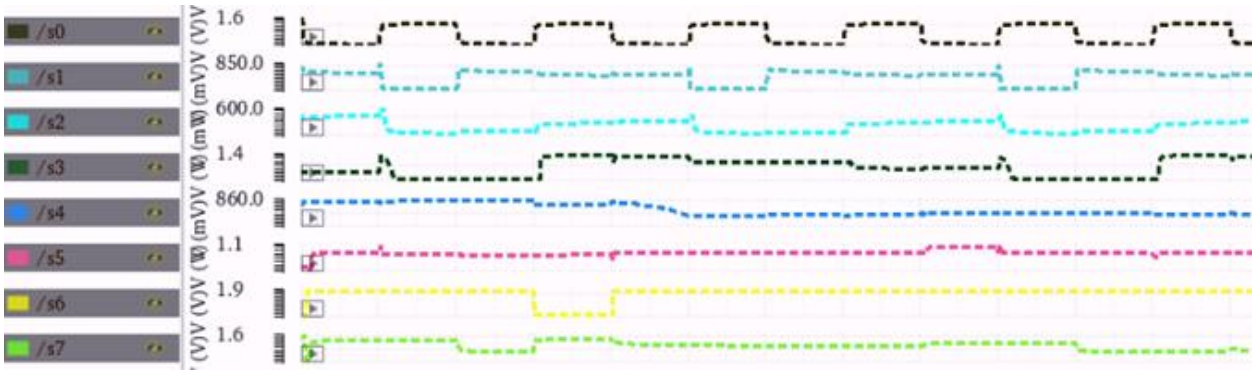

Fig: 12 output waveform of 4 bit multiplier

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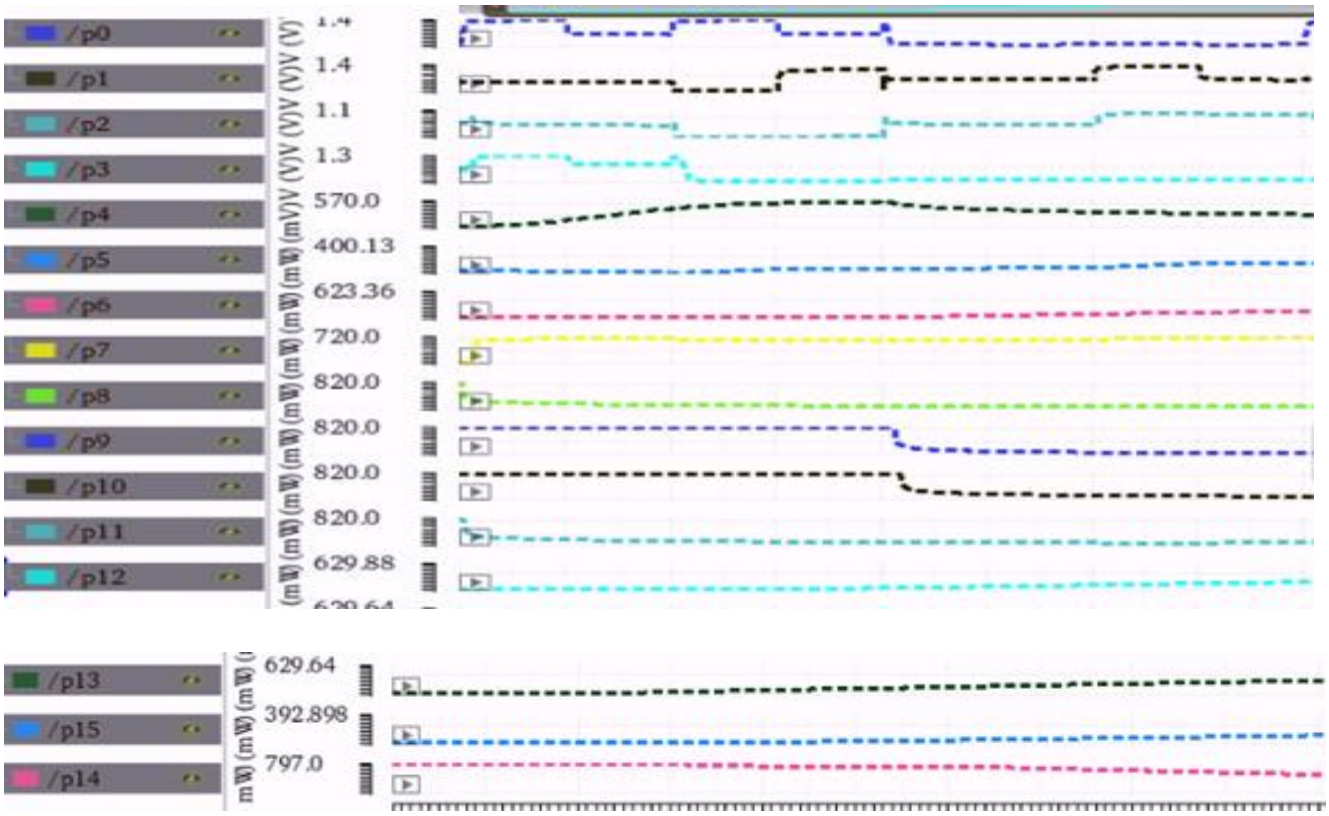

Fig:13 8 bit multiplier output

6. Conclusion

In this paper the concept of Vedic multiplication and GDI logic are used to design a 8 bit Vedic multiplier. The advantages of Vedic multiplication over the conventional multiplication and GDI logic over the CMOS logic are observed. In the results parameters like power, delay, TC is less in proposed multiplier when compared to the conventional multiplier design. The proposed multiplier simulation is are done using cadence tool. In future the GDI based multiplier design will be help in designing of FFT systems and also floating point multipliers design.

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