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Fin-FET based power optimized and latency improved decoder design using 7nm

[1]Thoram Saran Kumar, [2]Dr. Jagadeesh Bodapati

[1]Ph. D Scholar, Dept. of E.C.E, NIILM University, Kaithal, Haryana.

[2]Guide, Assistant professor, Dept. of E.C.E, NIILM University, Kaithal, Haryana.

ABSTRACT: Two efficient decoders designs with a novel selective precharge circuit have been proposed in this paper using 7nm FinFET technology. Back end designing in VLSI is a very important topic of research as the need of low power devices is in high demand, it is necessary to take action on circuits to reduce the power consumption from initially used conventional circuits. Decoder is an important circuit in the field of electronics and communication. Initially, CMOS logic is used for making decoder which utilizes 20 transistors and in mixed logic, same logic can be created using 14 or 15 transistor, but power consumption is still high. This thesis, FinFET based mixed logic line decoders for low power and high speed applications is proposed FinFET shows better results in terms of parameters such as Average Power Consumption, Delay, PDP and Voltage Source Power Dissipation. 2 to 4 and 4 to 16 decoders are made using MOSFET and FinFET Technology in 7nm.

Keywords: Decoder, FinFET, Short Gate, Power, delay; radiation induced single event transients; double-gate FinFET-based address decoder

INTRODUCTION: In recent years we are using CMOS technology for fabrication of IC's. The CMOS consists of both PMOS (pull-up network) and NMOS (pull-down network). This technology is used in fabrication of microprocessors, microcontrollers, static RAM and other digital circuits. In the applications such as image and signal processing, computer graphics, communication networks and digital applications the analog to digital and vice versa conversion is needed. To obtain these we are using encoding and decoding techniques. The encoding means the analog information is converted into binary form. The decoding means the coded value will be converted into original information. Based on types of applications different types of encoders and decoders are available.

To achieve low power and less area of encoder &decoder design we are using innovative MOS structures called Fin-FET technology. FinFET technology is also called as Double- gate CMOS (DGCMOS) is very close to that of conventional CMOS process, with only minor disruptions, offering the potential for a rapid devolvement to manufacturing. The benefit of finFET's double gate structure exhibits in the maximizing of the gate–to-channel capacitance and minimization of the drain-to-channel capacitances. In past four decades CMOS scaling has offered improved performance from one technology node to the next. This in turn has brought smaller and faster digital systems. However, future bulk CMOS scaling faces considerable challenges due to material ad process technology limits [1]. According to the 2011 International Technology Roadmap for semiconductors (ITRS) [2], obstacles to the increased scaling of bulk CMOS include short-channel effects, sub-threshold leakage, gate dielectric leakage, and device-to-device variations. These obstacles affect circuit and system reliability. The aforementioned challenges will become more prominent as CMOS scaling approaches atomic and quantum mechanical physics boundaries [3]. Efforts to extend silicon scaling through innovations in materials and device structure continue. FinFETs, which are double-gate field effect transistors, are able to overcome these scaling obstacles [2, 4]. One of the most important features of FinFETs is that the front and back gates may be made independent and biased to control the current and the device threshold voltage [5].

In VLSI technology, as we know that it contains thousands of transistors in a single chip called Integrated circuits (IC) with an increase in transistor densities by the law of Moore's, also increasing the power consumption with higher clock frequency. Now the trade occurs, where we try to make efficient logic circuits to optimize the key factors like Power loss, leakage current, voltage source, etc through which we can make the device more efficient with low power consumption. VLSI occupies a comparatively a low area. The size of the circuits is lessened.

LITERATURE SURVEY [1] D. Balobas N. this article introduces a mixed-logic line decoder framework consisting of door transmission logic, double-estate transistor logic and static CMOS. The 2-4 decoders display two story topologies: a topology with a 14-transistor pointing to limit the number of transistors and dispersion of energy and an topology of 15-transistors showing elevated energydeferment.. [2] Kazuo Taki, The review incorporates a few distinct perspectives, for example, circuit advancements, structure and amalgamation philosophies, applications and business use, and so forth. The circuit advancements and amalgamation strategies are generally assembled into two classes, one of which has a nearby connection to BDD, while different does not. Circuit advances are likewise classified into various tomahawks, For instance, differential or single-rail structure, NMOS or CMOS, static or dynamic circuit, and so forth. Along with these tomahawks classification, the highlights of each pass transistor logic family are explained. [3] Pooja Verma, This paper covers the two of these, the decoder and the multiplexer. In this work, planning of 2:1 MUX and MUX Based Decoder utilizing SCL (Source Coupled Logic) is finished. Power and estimation of current spike (Rail– to-Rail current) is found for the circuits. The Simulation is finished utilizing 180nm technology utilizing TANNER (Version 9.2) apparatus. [4] B. Madhuri, "This undertaking covers a mixed-logic line decoder design, gate logic, dualesteem pass transistor logic and static CMOS. The 2-4 decoders show two epic topologies. Finally, a wide range of relative zest recreations at the 32 nm shows that in virtually all instances the suggested circuit shows a remarkable increase in strength and delay. [5] D Komali, "This article introduces a strategy of a blended logic framework, combining the dual esteem logic transistor, transmission gate logic and the integral metal oxide haliconductor static structure approach. This shows that the circuits suggested have significantly improved energy and postponement, which in almost all instances are defeating CMOS.

Decoder using Fin-FET: NOR-BASED DECODERS: The NOR-based decoder has P-type transistors in the pullup network, termed as the precharge circuit which is activated to charge the word select lines. Depending on the applied address bits the N-type transistors in pull-down network discharge all select lines except the one which is to be selected, as all the transistors of that line are

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in OFF state. The precharge transistor is fed with the active-low clock pulse. When the clock pulse goes high, evaluation phase starts and only one select line remains charged in this phase [7], [8]. This can be observed from Fig.1 clearly. So we can say that a number of short circuit paths are always available between the supply and the ground terminal through pull-down network, because

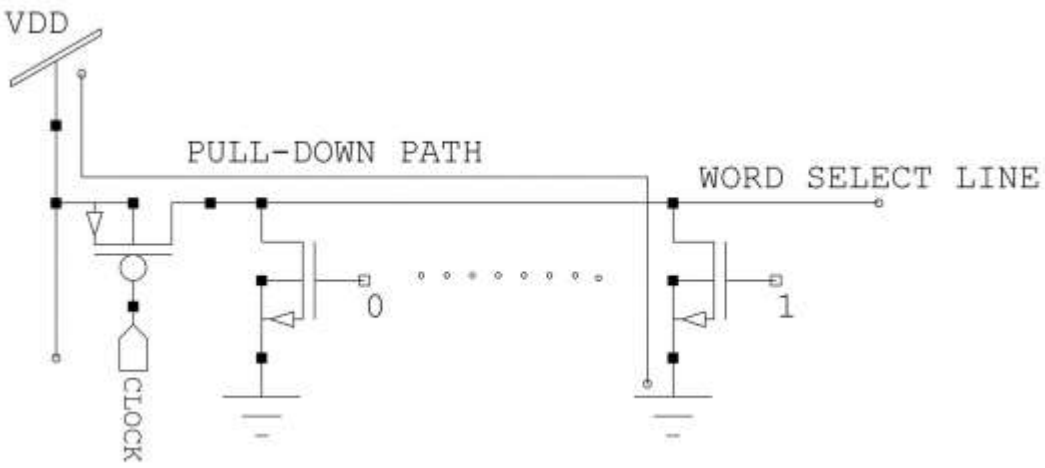

Fig 1: Basic NOR Decoder Operation

for any given address bit combination, only one select line will have all pull-down transistors OFF, rest all word lines will have at least one pull-down transistor ON. This is a major drawback of basic NOR-based decoder as it results in a huge amount of power consumption. To address this issue, designs were proposed in [7]–[10], but they add transistor overhead and make the circuit slow. Conventional 3:8 NOR decoder circuit is simulated using 32nm CG-FinFET technology in this work. The delay and average total power consumption of the circuit have been listed in TABLE III. Delay here is quantified as the time elapsed between the instants when the clock signal falls to 50% of VDD and the select line which is to be selected gets charged to 50% of VDD. Average total power is quantified as the product of supply voltage i.e. 0.9 volts with average current drawn from VDD terminal over the period of one clock cycle. The gate level schematic of the circuit is given in Fig.2.

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Decoder Design Using CG-FinFET: The continuous short circuit paths between the supply and the ground through pull-down network are the primary cause for huge power consumption in the basic NOR-based decoders. A better choice is there to connect selectively only a few of the word lines to the supply while other select lines remain discharged and isolated from the supply [7]. To address this issue, a novel precharge circuit based decoder is proposed. In this decoder circuit, extra PFinFETs are introduced in the pullup network. These PFinFET are driven with most significant bits (MSB) of the address. Fig.2 shows a 3:8 NOR decoder with proposed selective precharge scheme using common gate FinFET. a0, a1 and a2 are the address bits. out0, out1 to out7 are the word select lines. 1 GHz pulse is applied as the clock-pulse. When the clock-pulse goes low it turns on the first PFinFET connected to select lines. Out of 3 address bits 2 MSB's i.e. a2 and a1 are used to drive next two precharge PFinFETs connected to the select lines.

TABLE1: Truth Table of Proposed Selective Precharge Circuit

a_2	a_1	Select Lines Connected to Supply
0	0	out0, out1
0	1	out2, out3
1	0	out4, out5
1	1	out6, out7

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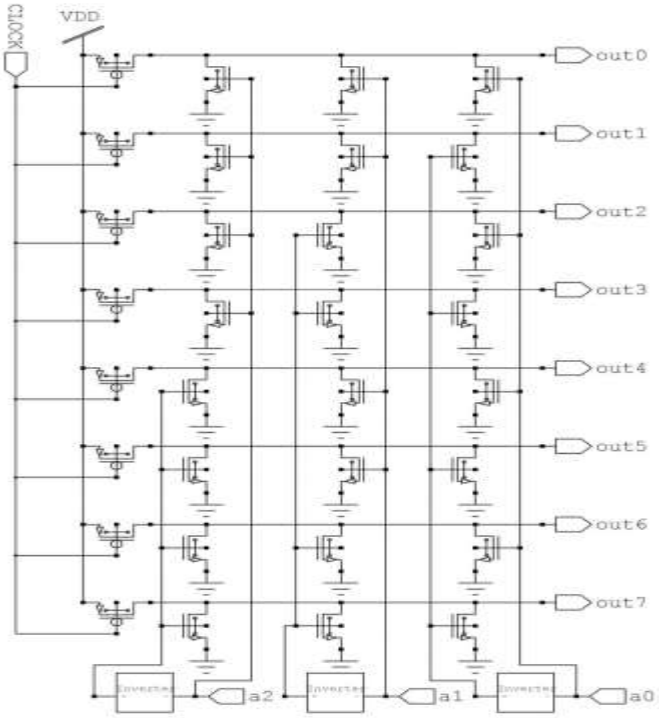

Fig.2: 3:8 NOR Decoder Schematic using CG-FinFET

Total four combinations are possible from these two bits. In this way for any combination of address bits, only two out of eight word lines given in Fig.2 are charged, rest six word lines remain discharged. This can be seen from TABLE I. Moreover all the short circuit paths in these six word lines are eliminated which results in a significant reduction in total average power consumed. As extra transistors are added in the circuit so there is a slight increment in delay of the circuit .

Decoder Design Using IG-FinFET: Process variations are the result of unavoidable errors born during the fabrication process. As we move further into the deep sub-micron regime, process variations assume greater importance, since integrated circuits (ICs) become more sensitive to parametric variations [4], [5]. This is because the parametric dimensions of the devices like Gate Length (LG), Oxide thickness (Tox) and channel width (W) become comparable to the wavelengths of lights used in lithography processes. This results in random variations in the designed parameters which reflect as a less reliable device as the electrical parameters depending on these parameters

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listed above also become random. So in order to make a circuit more reliable, some circuit level techniques must be employed. To observe the process variation effects on the conventional NOR-based decoder design, the circuit given in Fig.3 has been simulated using Tanner EDA runs and the delay variations have been tabulated. The standard deviation has been

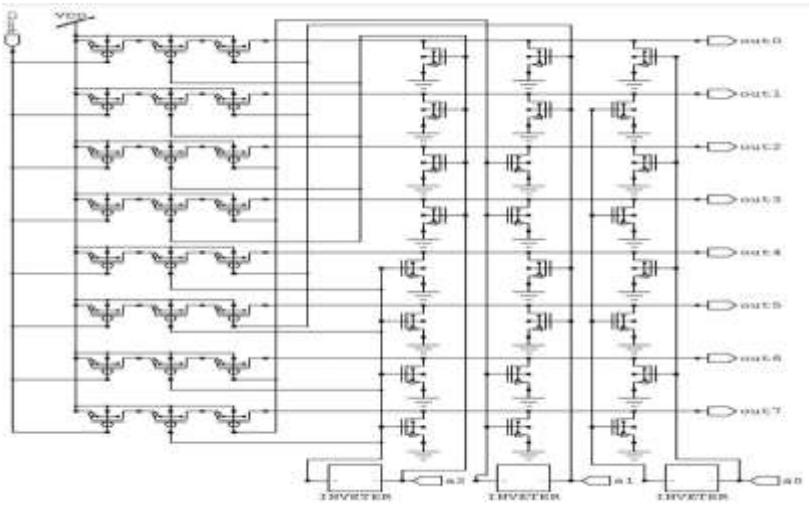

Fig. 3: Proposed Decoder Circuit using CG-FinFET

found to be 4.19 for the mean delay of 19.98ps. In order to suppress these variations, CG-FinFET is replaced with IGFinFET in proposed decoder circuit [6]. The schematic of proposed decoder with IG-FinFET is given in Fig.4. In IGFinFET we can operate the device as per requirement by applying suitable back gate bias voltage. Reverse bias on the back gate increases the threshold voltage of the device which reduces the sub-threshold leakage and also stabilizes the variations in delay due to process variations. A reverse bias of 0.4 volts on both PFinFET and NFinFET has been applied, and the circuit was simulated using same Tanner EDA runs. The delay variations due to process variation effects found to be suppressed to a large extent. Leakage power also got reduced due to the reverse bias applied to back gate.

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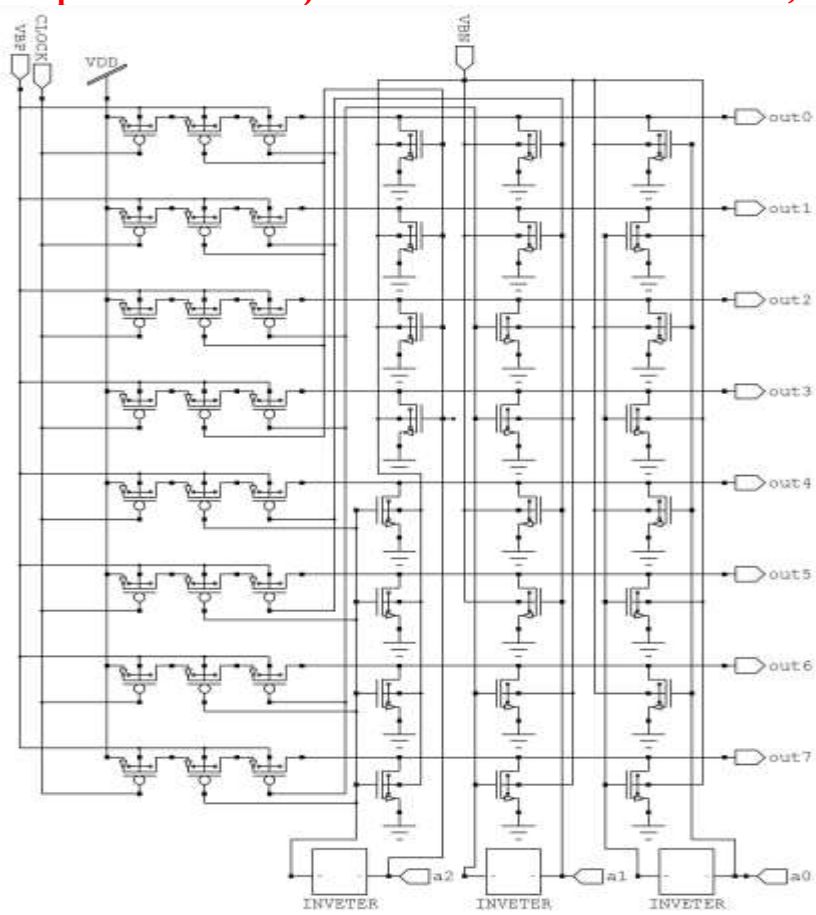

Fig. 4: Proposed Decoder Circuit using IG-FinFET

RESULSTS

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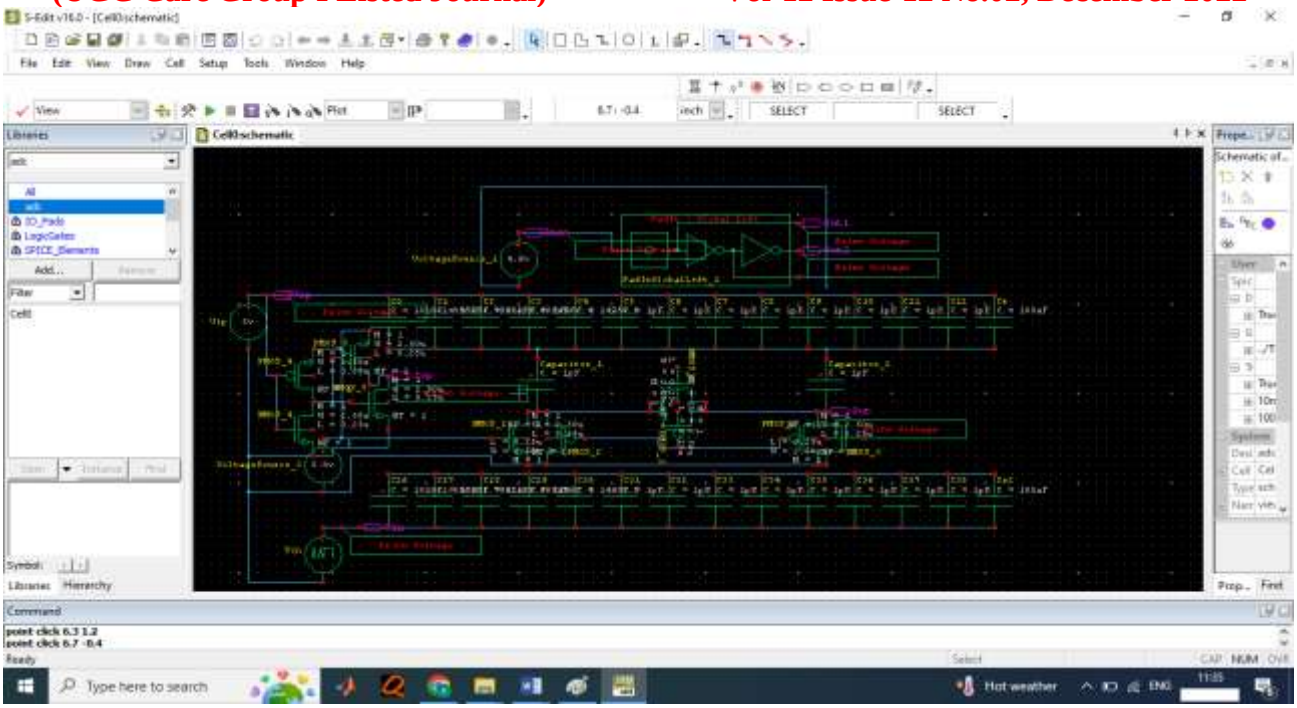

Fig5 Decoder schematic design

Above snap represents over all 3:8 decoder architecture taken in tanner EDA tool with 2V as operating voltage.

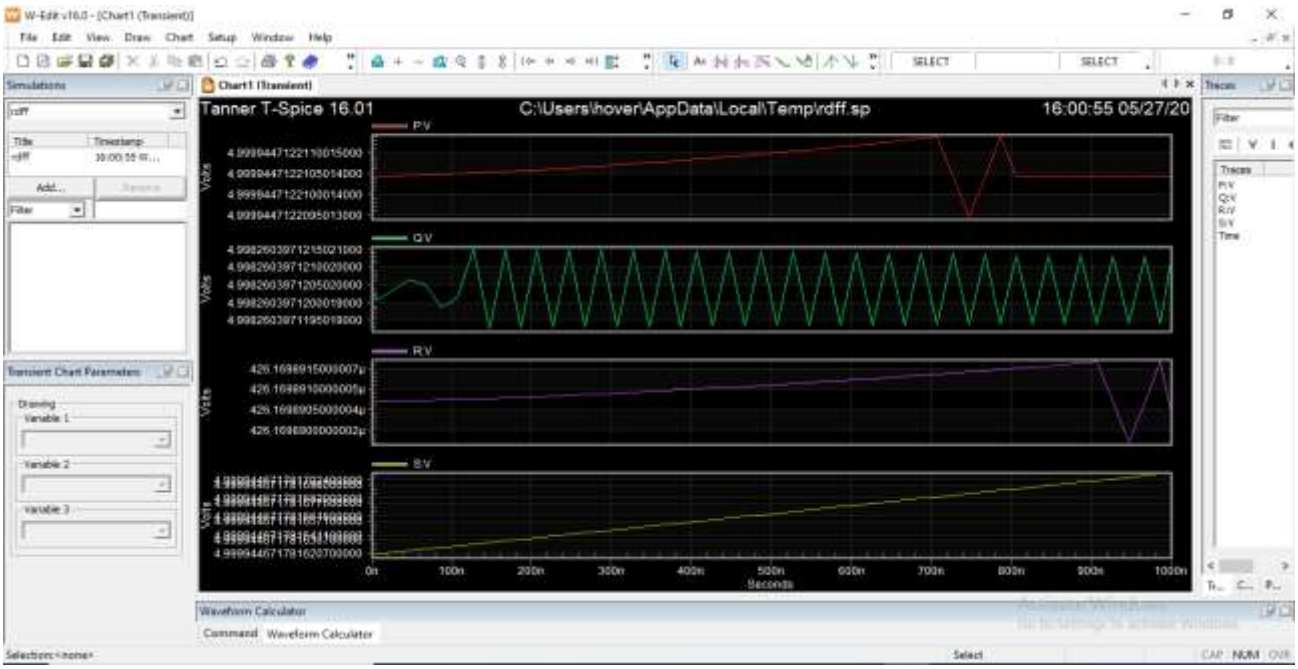

Fig:6 Decoder simulation output combination1

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Above simulation results shows 3:8 decoder with input combination as all ones. i.e all inputs are assigned to 5 V source.

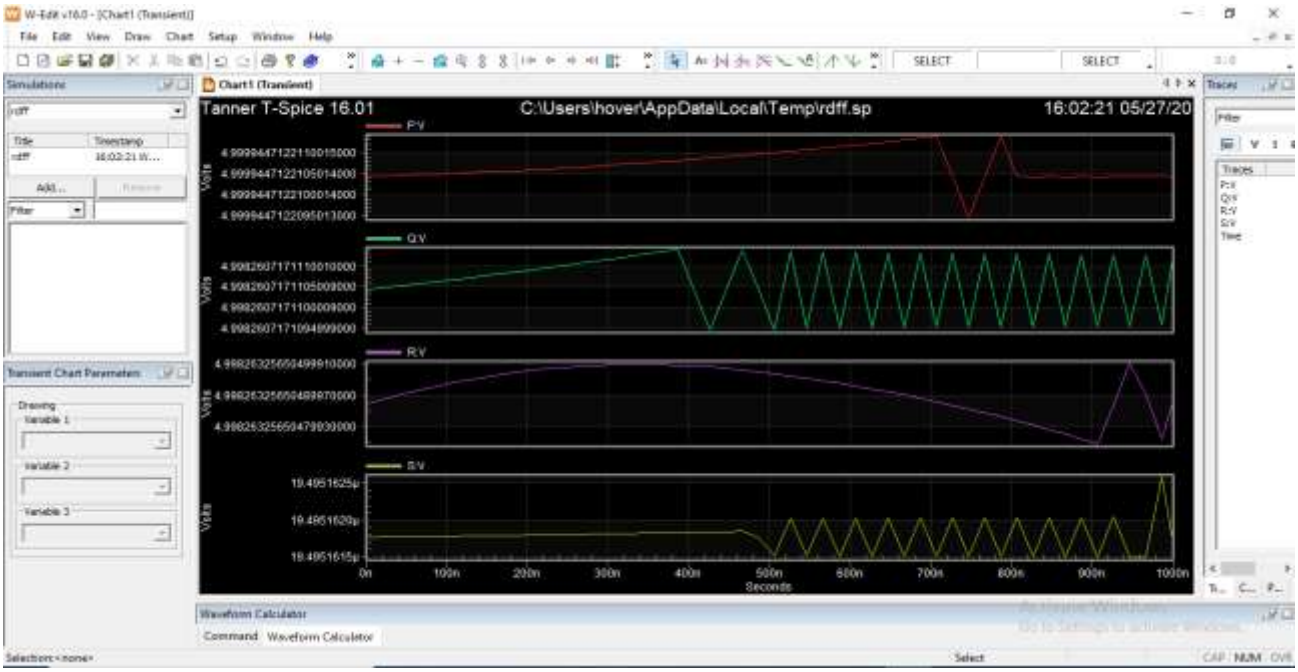

Fig:7 Decoder simulation output combination2

Above simulation results shows 3:8 decoder with input combination as all ones except final input. i.e all inputs first 2 inputs are asserted with 5v. Last input is asserted with 0V.

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Fig:8 Decoder simulation output with all combination

Above simulation results shows 3:8 decoder with input all combination. Taken as timing diagram for given design decoder.

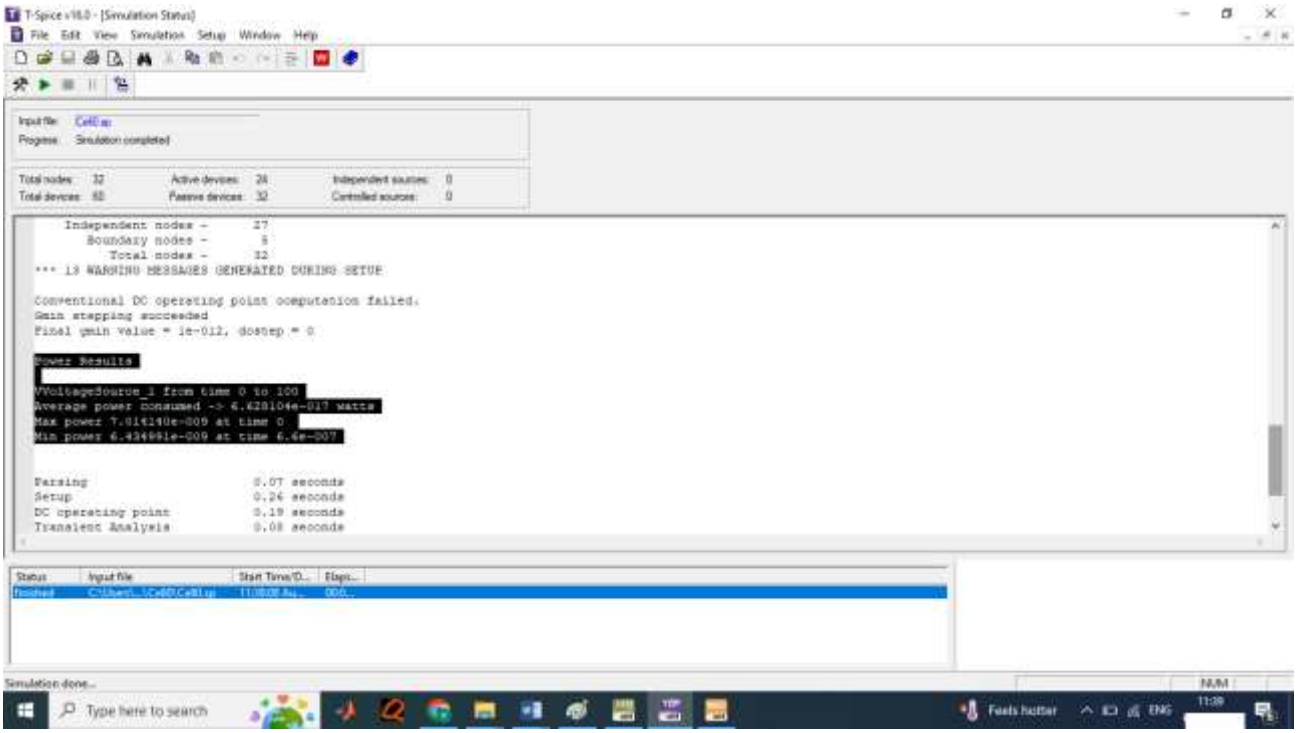

Fig9 Power report

Above synthesis results shows 3:8 decoder power consumption report with total average power consumption as well maximum peak power consumption.

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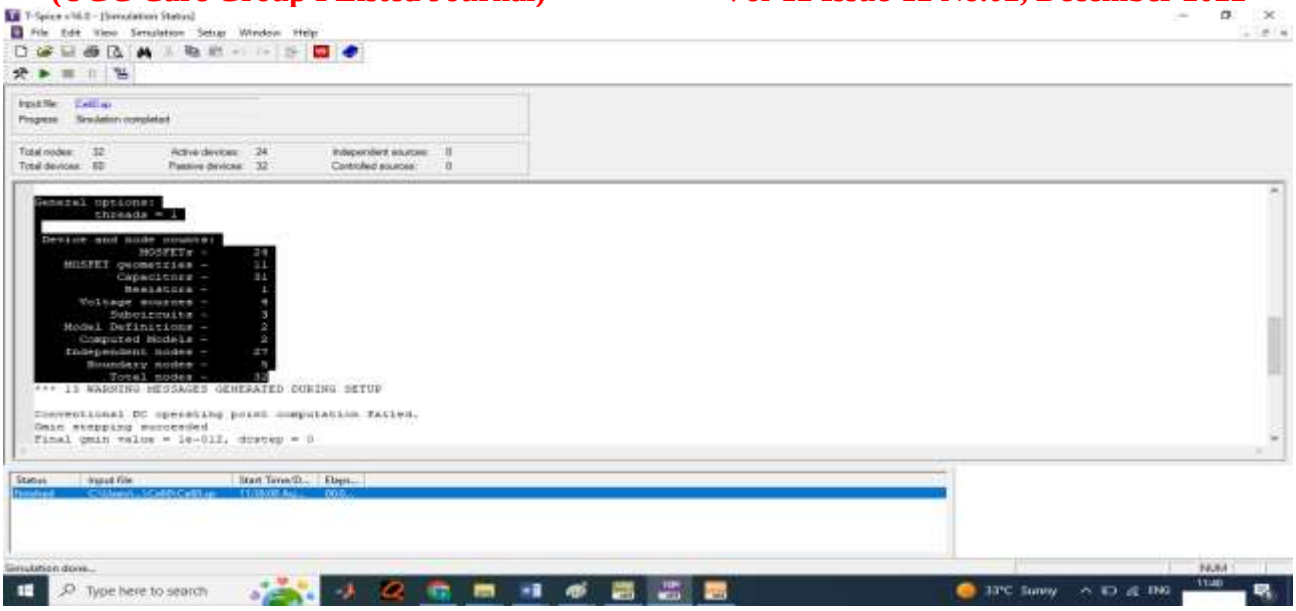

Fig10 Device utilization report

Above synthesis results shows 3:8 decoder area utilization report in terms of transistor count and power sources.

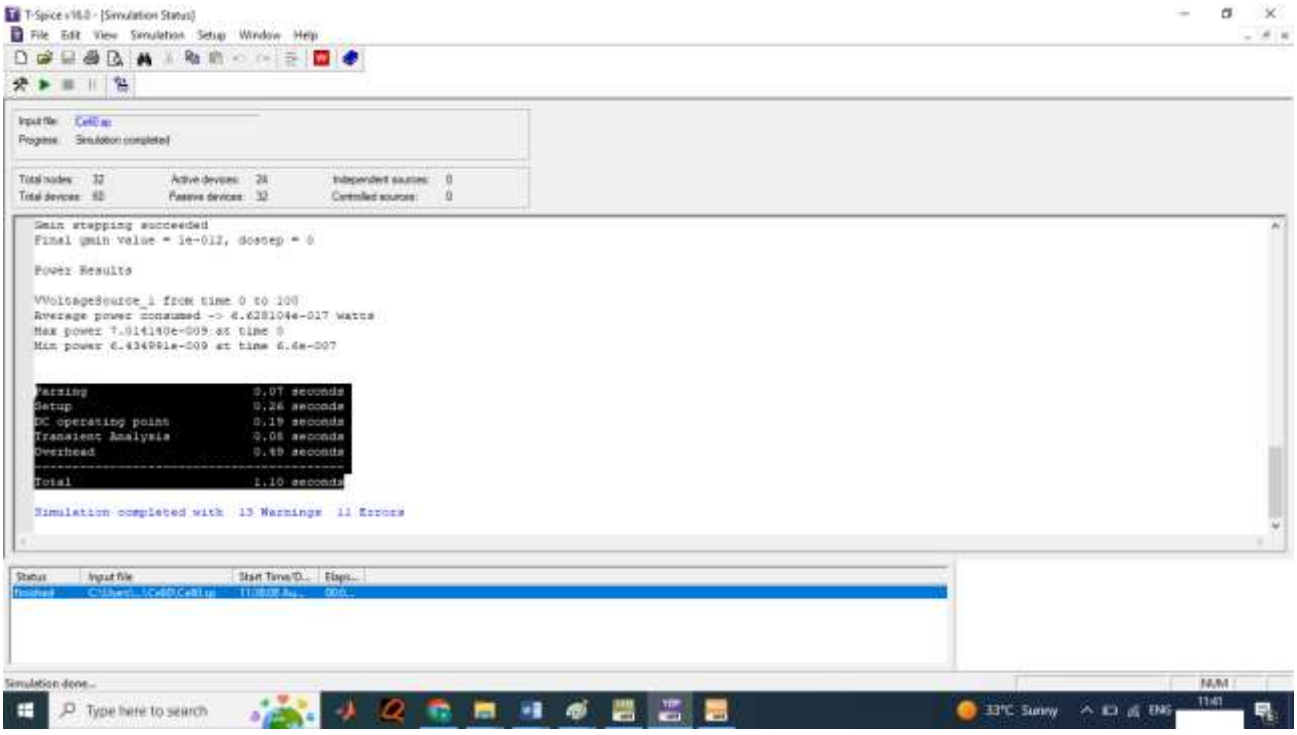

Fig:11 Timing Summery

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Above synthesis results shows proposed 3:8 decoder maximum combinational path delay in seconds.

TABLE2: Comparison of Delay and Power of Conventional and Proposed Decoder Schemes

Decoder Scheme	Delay (ps)	Average Total Power (μWatts)	Power Delay Product (fJ)
Conventional Decoder with CG-FinFET	12.3	2262	27.82
Proposed Decoder with CG-FinFET	19.98	142	2.83
Proposed Decoder with IG-FinFET	22.7	126	2.86

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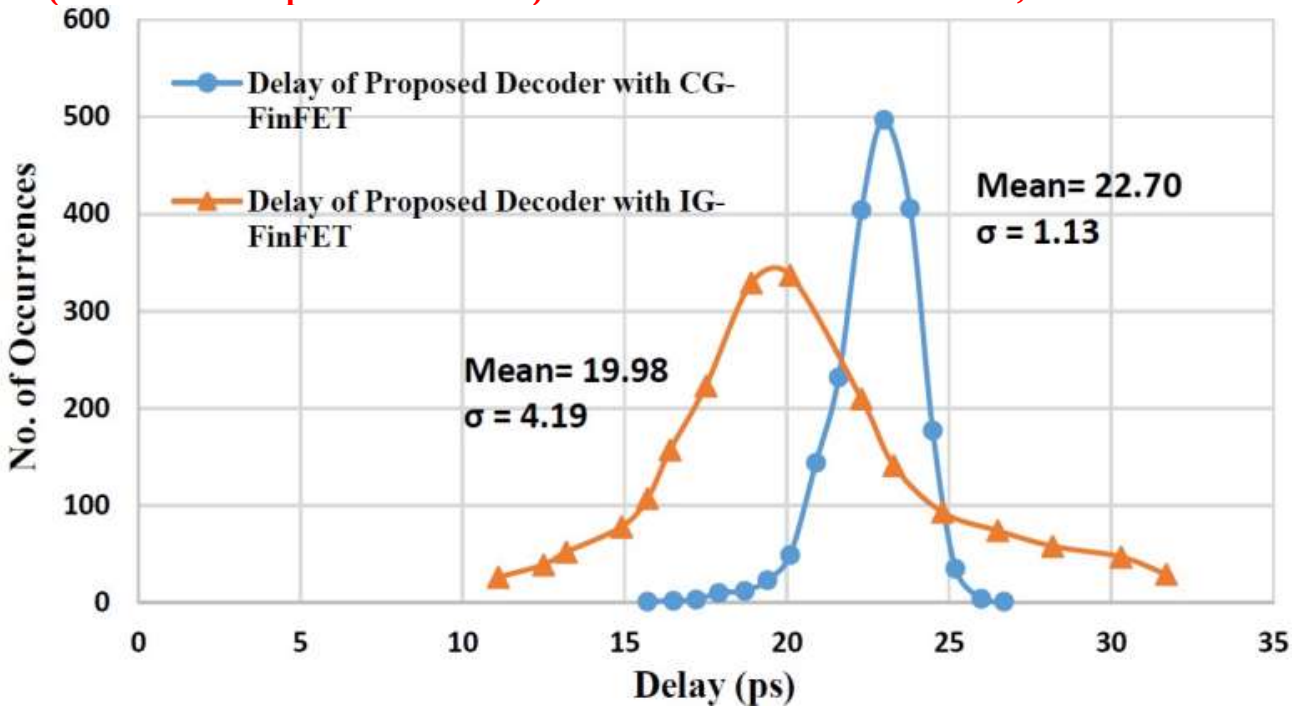

Fig. 12: Process Variation Effects on Delay of Conventional and Proposed Design

CONCLUSION:

This research proposes 2 innovative decoder schemes using CG-FinFET and IG-FinFET technology. The first scheme uses a novel selective Precharge circuit which reduces the total average power consumption by 93% at the cost of slight increment in delay from 12.3ps to 19.9ps. The second decoder scheme uses independent gate mode of FinFET along with a reverse bias applied to the back gate. This reduces the leakage of the circuit by 11.26% and variations in delay due to process variations are suppressed by 68.76% as the standard deviation (σ) is brought down to 1.13 from 4.19. This is achieved at the cost of a very little increment in circuit delay from 19.9ps to 22.7ps, which is a negligible change. Thus these designs can be a promising decoder option for low power memory designs in high-speed processors.

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