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Design of Multilayer ALU Using Landauer Clocking in Field coupled Nano Technology.

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***Abstract*—Quantum dot cellular automata is a field coupled nanotechnology which is an alternate to the transistor based technology(CMOS). The Transistor based technology has some limitations such as high power density levels, high leakage currents, high lithography costs.Thus, in order to overcome these problems QCATechnology has been chosen. It uses a Lauder clocking scheme to provide better performance.The Arithmetic Logic Unit (ALU) is the basic chunk for the digital computers sequenceto execute eight arithmetic & four logical operations. In which multiplexer and full adder plays a prominent cameo to perform the operation.Thus we proposed a new low complicacy 4:1 multiplexer and full adder based on the Coulomb repulsion. Based on these structures a one bit multilayerALUis designed.Hence the proposedstructure will apply to even more complex systems. Moreover these structures are fiture in a QCA designer tool 2.0.3 version. The aim of the project is to diminish the area, power dissipation, delay and increase the speed.**

Keywords—Quantum dot cellular Automata,Lauder clocking, Arithmetic Logic Unit(ALU),Multiplexer,Full adder.

I. INTRODUCTION

Transistor based technology (CMOS) [1] is a reputable machinery which is utilized in the arrangement of very large scale integration circuits.It has unnamed limitations such as high leakage current, power thermal, high cost, manufacturing process complexity increased, degradation of speed due to scaling. Thus in order to overcome these limitations QCA is a contemporary procedure to analyse and perform eminent digital circuits at nano scale. Itis the field coupled nanotechnology which replaces the bulkcmostechnology. It has numerous advantages such as small featured size at the molecular,area occupied by the circuit is less. In 1993 Lent and Tougaw inaugurated the QCA which serves the neighboring cells based on the coulomb repulsion. Hence, QCA is classified into three categories such as a metal QCA, molecular QCA, magnetic QCA.We considered a molecular QCA in which this method includes a square pattern QCA cell with four charged containers are known as quantum dots. Unlike in the typical computers in which data is conveyed from one deposit to another by providing electrical current. Where as in QCA there is no need of electrical current Thus, the data is fetched from one cell to another based on the polarization state. HenceBased on the polarized state the binary operation is considered.Landauerclocking is most common scheme used in QCA.

Arithmetic and logic unit is the basic component for the digital computer sequence to enactarithmetic and logical operations. In this paper a new low complicacy 4:1 multiplexer and full adder is designed. Thus based on these structures one bit multilayer ALU is implemented to perform twelve operations which includes 4 logical and 8 arithmetic operations. The main aim of the project is to increase the speed and diminish the area and power dissipation. Proposed structures widen its applications over optical computing, quantum computing.

The rest of this concise is catalogued as below: Overview of QCA, clocking in QCA is shown in vicinity 2. The affirmed formation of 4:1 multiplexer and full adder is shown in vicinity 3.In vicinity 4the affirmedmultilayer one bit QCA ALU is shown. In vicinity 5 Simulated wave forms are shown. Conclusion of our project is shown in vicinity 6.

II. OVERVIEW OF QCA

A. QCA CELL

QCA has unbelievable eventual to oust the cmos technology. QCA is implemented by a quadratic cell called QCA cell. A square pattern cell repose of four aluminum metal dots which are known as quantum dots .These quantum dots are situated at corner of the cell. In which they aresurrounded by a insulating material. InQCAthe data is fetched from one cell to another based on the polarization state. Hence due to the polarization state the binary operation is considered.The localized electrons will occupy diagonally or 45 degrees based on the coulomb repulsion thus, it is much efficient than the electrons which are located adjacently.These electrons are connected through a tunnel junctions.

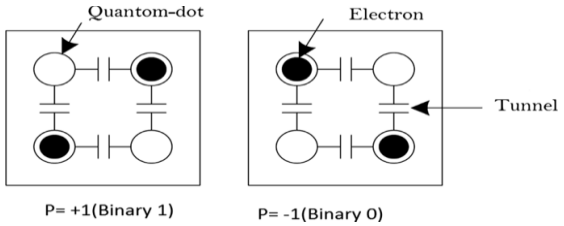


Fig 1. Representation ofQCA Cell.

In QCA, the binary operation is carried out by the spin of localized electron within a cell.Based on the polarized states the binary operation is considered.Further QCA cell is completely polarized state known as cell polarization.It is denoted as p=+1 which will be represented as ‘1’ in binary and p=-1 is considered as ’0’ in binary as shown in figure 1.

ISSN: 2278-4632
Vol-10 Issue-5 No. 7 May 2020

B. Clocking in QCA.

In QCA the clocking is not a separate wire which will be bolster into a circuit .It is the cyclically explore to be aelectric field which checks potential barrier within a cell. Clocking mechanism shows a vital cameo in a QCA circuit which provides a power gain and to make sure that QCA cell won't resolve into a meta stable state .so in order to prevent from the meta stable states clocking is important.There are four colors of clocking zones in which individual zone has an unique colour.Thus, four clock zoneis known as landauer clocking .The four clock zones are shown in figure 2.

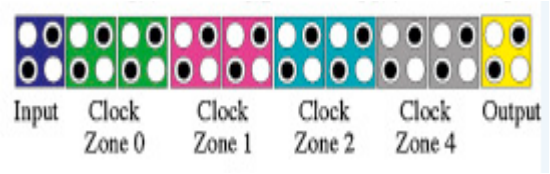


Fig. 2. Representation of Four Clock zones.

If all zones having same color then it receives the same color phases at the same time. In clocking mechanism which includes Switch, Relax, Hold, and Release phases [2] .In first (switch) phase the tunneling barrier start to rise and the cells become polarized with respect to the state of input cell. The second (hold) phase stretched to the tunneling. In third (release) phase tunneling barriers are lowered.Finally, the fourth (relax) clock phase cells remain unpolarizedstate. The four clock phases are shown in figure 3.

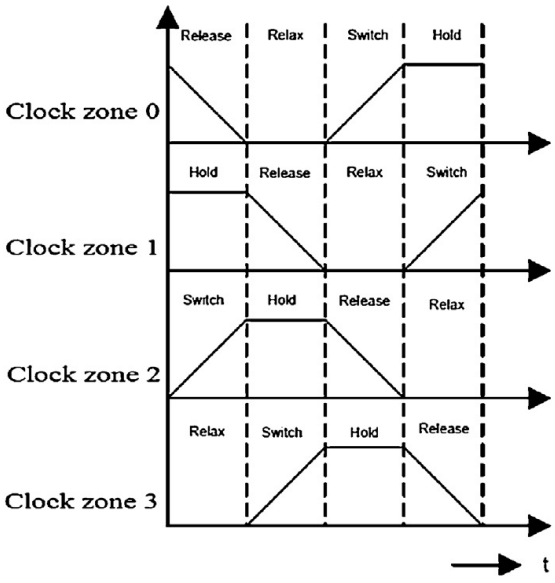


Fig. 4. Four phases of clock zone.

IIIPROPOSED QCA STRUCTURES.

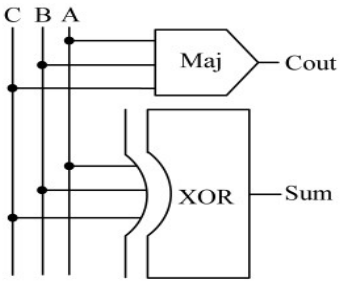
A.Arrangement of a Full Adder

Full adder is the prominent basic component used in the arithmetic operations[3] it performs not only sum operation but also other arithmetic operations such as multiplication, divisionandsubtraction. We used majority gate along with XOR gate to implement a full adder. There are three inputs such as A,B &Cin. Thus, it generates the two outputs sum and carryout. These can be estimatedby equation 1 and equation 2.

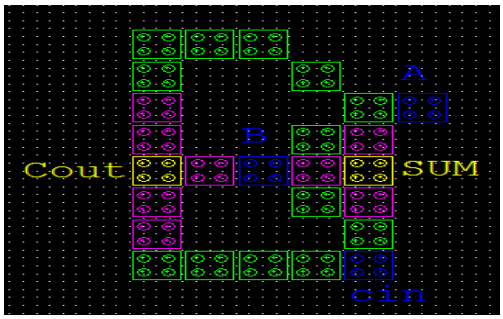
$$Sum = A \oplus B \oplus Cin \quad (1)$$

$$Carryout = AB + BCin + CinA = M(A, B, Cin) \quad (2)$$

Here 'M'denotes majority gate.The output is produced based on coulomb repulsion. The urged structure includes majority gate and XOR gate.



(a)



(b)

Fig.5Full adder structures (a) Logical setup (b)circuit.

B . Affirmed multiplexer for arthimetic unit

The Arithmetic and logical operations are shown in table I .There are eight arithmetic functions in which the sum operation is fixed for all eight functions. Thus, all the arithmetic operations are easily performed with designed full adder. In four cases when Cin is '0' then the operation will have addition with '0'.If Cin is equal to'1' then the sum remains with '1'. Whereas the value 'A' along with addition of input Cinis hookedfor all eight arithmetic operations.In which they are directly joined to full adder. Removingvalue'A' additionwith respect to '0' and addition with respect to'1'from tableI, leftover values are shown in table II which are inputs of full adder.

TABLE I. OPERTAIONS OF QCA ALU

Operations	Mode	S1	S0	Cin	Out

ISSN: 2278-4632
Vol-10 Issue-5 No. 7 May 2020

Logical	0	0	0	×	A⊕B
	0	0	1	×	A^ B
	0	1	1	×	A∨ B
	0	1	1	×	A'
Arithmetic	1	0	0	0	A
	1	0	0	1	A+1
	1	0	1	0	A-1
	1	0	1	1	A
	1	1	0	0	A+B
	1	1	0	1	A+B+1
	1	1	1	0	A+B'
	1	1	1	1	A-B

.

TABLE II. REPRESENTATION OF FULL ADDER

S_1	S_0	Out
0	0	0
0	1	1
1	0	B
1	1	B'

S_1 \ S_0	0	1
0	0	1
1	B	B'

(A)Truth table (B) K-map

The urged 4:1 multiplexer is made to show the familiar output. Moreover, the output of 4:1 multiplexer is given by equation (3).

$$Y = [(\overline{S1}\overline{S0} \times 0) + (\overline{S1}S0 \times 1) + (S1\overline{S0} \times B) + (S1S0 \times \bar{B})]$$
$$= [(\overline{S1}S0) + (S1\overline{S0}B) + (S1S0\bar{B})] \quad (3)$$

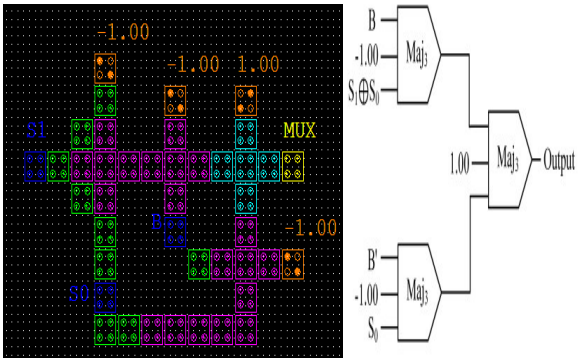
The output arrangement of multiplexeris in the sum of product of canonical form. Therefore above equation can be rewrite as

$$Y = [(\overline{S1}S0 \times (B + \bar{B})) + (S1\overline{S0} \times B) + (S1S0 \times \bar{B})]$$

From the above equation, it can be modified as shown in equation 4.

$$Y = [B(\overline{S1}S0 + S1\overline{S0} + S0\bar{B}(S1 + \overline{S1})] \quad (4)$$

The proposed 4:1 multiplexer is based on equation 4..Here we considered three majority voters. The QCA layout and logical diagramis delineated in figure 6.



(a) (b)

Fig. 6 (a) circuit(b) Logical setup of 4:1 Multiplexer

C . Affirmed multiplexer for logical unit.

It perform operations such as AND,XOR,OR and NOT .This unit is implemented based on the coulomb repulsion.

$$Y1 = [\overline{S1}\overline{S0}(A \oplus B) + \overline{S1}S0(AB) + S1\overline{S0}(A + B) + S1S0(\bar{A})] \quad (5)$$
$$= \overline{S1}\overline{S0}\bar{A}B + \overline{S1}\overline{S0}A\bar{B} + \overline{S1}S0AB + S1\overline{S0}A + S1\overline{SO}B + S1S0\bar{A}$$

Equation 5 can be simply modified as follows in Equation6.

$$Y1 = S1S0\bar{A} + \overline{S0}\bar{A}\bar{B} + \overline{S1}\overline{S0}A + \overline{S1}\bar{A}(S0 \oplus \bar{B}) \quad (6)$$

It shows that equation 6 is designedfor the logical unit of proposed ALU structure.

IV IMPLEMENTATION OF QCA ALU STRUCTURE.

ALU is most important or all the digital computers sequence to executearithmetic and logical unit.The operations like sum, subtraction,multiplication, division are performed by arithmetic unit. logical unit performs NOT,AND and OR. In digital computers binary data is represented in 16, 32 and 64 bit quantities.Thus we considered a 1 bit quantities to design a circuit. Further the proposed QCA ALU is applicable for quantum computing,DNA mapping.The logical diagram and layouts are shown in figure 7 and 7.1 respectively.

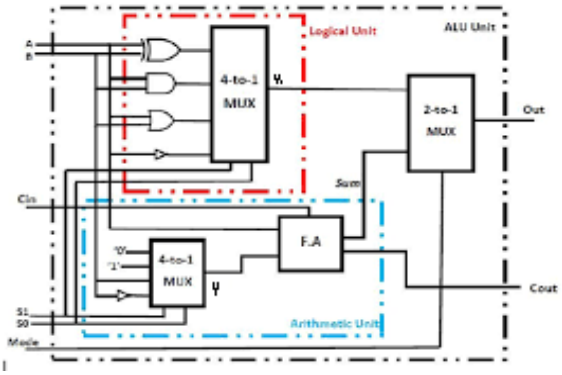
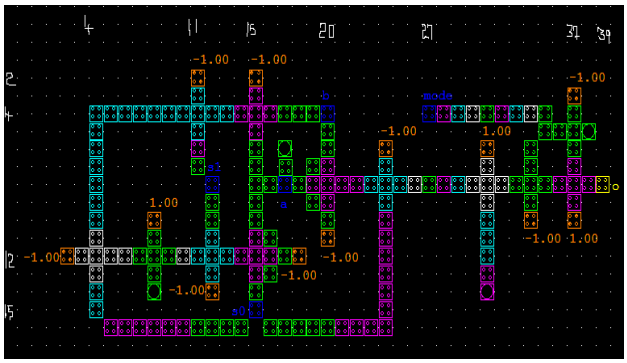
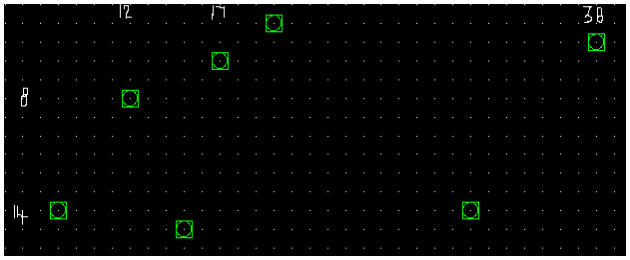


Fig 7. Logical setup of QCA ALU

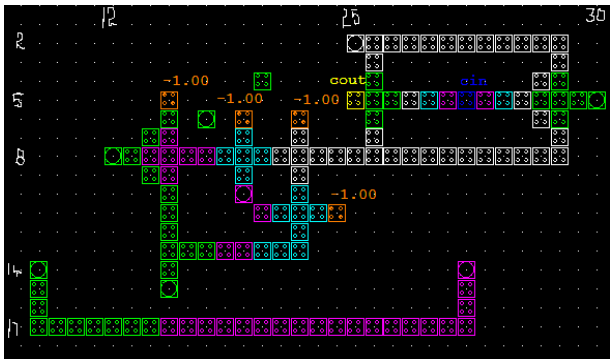
ISSN: 2278-4632
Vol-10 Issue-5 No. 7 May 2020



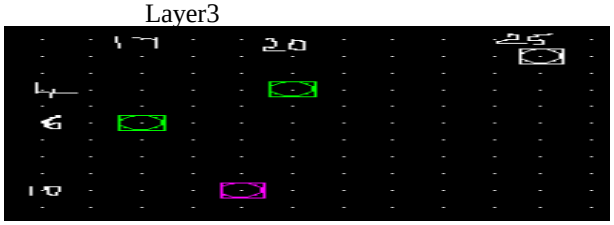
Layer1



Layer2



Layer3



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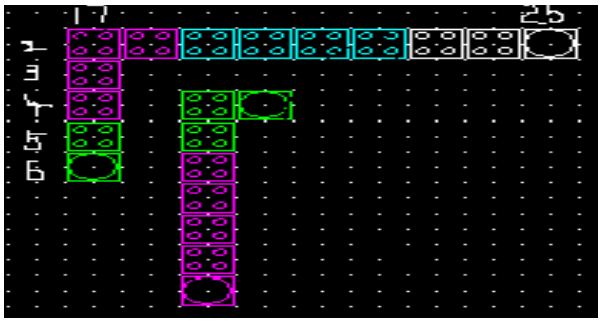


Layer5

Fig7. Layout of one bit multilayer ALU.

V SIMULATION RESULTS.

The urged scheme are evaluated by the QCADesigner version 2.0.3 in which clock rate is 1Thz.QCA is opted to reduce the clock latency area and power consumption.

In TableIII, TableIV & TableV shows that 4:1 multiplexer and ALU are correlated with the peer architectures.The contrast shows thatstipulation of area, cell count, and latency.

TABLE III. COMPARION OF VARIOUS QCA FULL ADDER.

Full adder designs	Cell count	Area (μm^2)	Clock cycle
[4]	35	0.0288	1
[5]	33	0.02	0.5
[6]	53	0.047	0.75
[7]	41	0.03	4
[8]	46	0.04	4
Proposed structures	26	0.03	0.5

TABLE IV. COMPARION OF VARIOUS SINGLER LAYER 4:1 MULTIPLEXERS.

4:1 Multiplexers designs	Cell count	Area (μm^2)	Clock cycle
[9]	61	0.08	4
[10]	107	0.15	1
[11]	107	0.17	5
Proposed structures	42	0.07	1

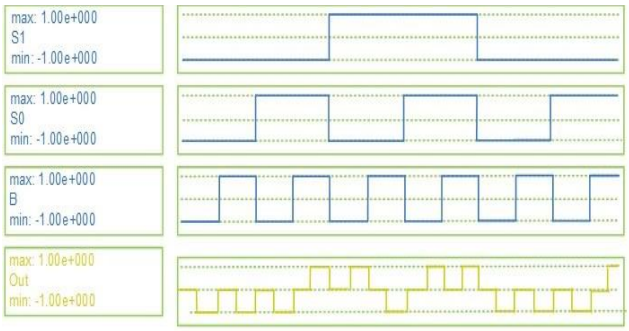
TABLE V. COMPARION OF VARIOUS QCA ALU.

ALU designs	Cell count	Area (μm^2)	Clock cycle
[12]	12	0.624	N/A
[13]	4	0.78	3
[14]	5	0.76	5
Proposed structures	12	0.245	2.25

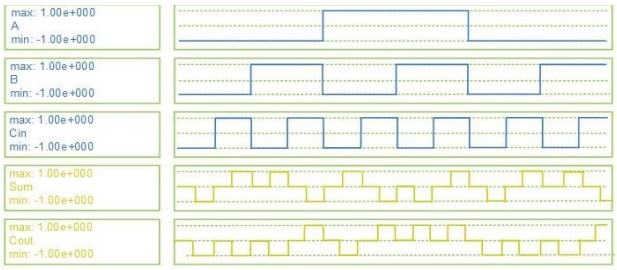
A . Structural analysis

In the bi stable simulation considered to analyse the proposed designs. Thus simulation results of 4:1 multiplexer, full adder and one bit multilayer ALU is shown in figure 8(a),8(b),8(c).

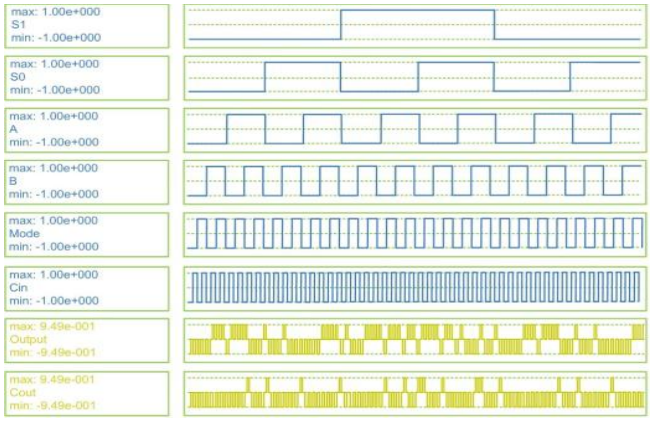
ISSN: 2278-4632
Vol-10 Issue-5 No. 7 May 2020



8(a)



8(b)



8(c)

Fig 8.Simulaed waveforms (a) 4:1 multiplexer (b) full adder (c)one bit ALU.

VI CONCLUSION.

In this paper multilayer one bit ALU is designed.The Arithmetic Logic Unit (ALU) is the basic chunk for the digital computer sequence to enact arithmetic and logical operations.In which the affirmed ALU performs eight arithmetic and four logical operations, in which multiplexer and full adder plays a prominent cameo to perform the operation. Thus we proposed a new low complicacy 4:1 multiplexer and full adder. Thus multiplexer has 42 cells,0.06μm² area, &one clock latency. Where as in preceding implementations has 62 cells and four clock latency. By utilizing these basic QCA layouts a new efficient 1-bit multilayer is implemented in which it performs total 12 operations. The results shows that its area0.24μm²and 2.2 clock cycles. The designed ALU is applicable for digital computer, quantum computing and many more applications. Future extension is to reduce the area as well as to implement the two bit multilayer ALU.

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