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Detailed Analysis of Low Power Bulk driven Current Mirror

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Abstract

MOSFET has been the heart of the VLSI design from the last few decades till the present era. Physically it is a four terminal device but mostly only three terminals are being employed for practical applications. The bulk has been traditionally used as a substrate. Many approaches have been reported in literature for utilizing bulk as an additional control terminal in collaboration with the gate terminal. Now the theoretical aspects have classified MOSFETS basically as traditional SoI (Silicon on Insulator) MOS and Bulk MOS. From the operating point of view analysis in terms of region of operation among cut-off, sub threshold and saturation needs to be known prior to applications. Threshold voltage of MOSFET is the prominent parameter for turning the device on or off and depends on several factors such as bulk potential. This paper reviews the basic aspects of MOSFETS with respect to bulk terminal. A detailed analysis of effect of bulk potential on the characteristics of current mirror has been analysed. A tabular analysis in terms of transfer characteristics using parametric analysis of threshold voltage with variation of VGS (gate to source voltage) and VDS (drain to source voltage) has been presented using Cadence Virtuoso tool on the 180nm feature technology.

Keywords: ***MOSFET*, Bulk MOS, SOI MOS, Threshold Voltage, Bulk potential, current mirror**

Organization of paper is as follows. Section 1 describes introduction of basic MOSFET technology and description of SoI and Bulk MOSFET with threshold equations and mathematical analysis where needed. Section 2 briefly describes about the applications of low power devices with respect to MOSFET. Section 3 describes inverter based on bulk MOS and gate driven MOS and differentiates between the two approaches. Section 4 describes the current mirror designs and comparative analysis using Bulk MOS and SoI MOS concepts. Sections 5 is showing the detailed results of the above sections with the graphical representations mainly focussing on the graphical representation of the Bulk MOSFET characteristics, Inverter characteristics and Current Mirrors characteristics. Section 6 describing the conclusion of the study between Bulk and Gate Driven technology.

1. Introduction

Power consumption has become the major issue in today's world with the advancement of the technology. Portable smart devices like mobile phones, computers that are powered by batteries are the major reasons behind low power requirement. Another demand for low power chips and smart systems comes from environmental concerns with vision of energy conservation. Modern offices are now furnished with office automation equipment that consumes large amount of power. Low power VLSI devices find increasing application in portable devices, spaceships, computing devices etc. Demand for higher functionality and better performance at lower cost is the main motivation behind the continuous downsizing of CMOS based ICs. With the advancement in the submicron technologies which majorly involves the shrinking of transistor sizes and hence leading to higher density of components within the limited area. This eases the increment in operating frequencies and moreover the processing of chips is getting better in terms of performance. The major issue which arises with the large scale and ultra large scale integration is the heat generated due to power consumption by the transistors. In simple terms, when the transistor density increases in a specifically small area, the cumulative power dissipated by overall unit including millions of transistor raises an issue for the power dissipation domain. This power dissipation arises in the form of heat majorly on the chips and thus arises a need for low-power VLSI chips from such evolutionary forces of integration on circuits in today's era [1, 2].

In the present world, advancement in semiconductor technology and increasing performance based user friendly products; majorly the designs included for the systems are such as to integrate whole systems on a single chip. This can be seen from latest products such a wearable healthcare electronic products such as watches, mobile phones, migraine headache machine, and laser hair drier. Moreover, the explosive growth of mobile computing devices that are typically constrained by power consumption has brought hardware and software techniques for energy conservation into the spotlight [3].

The ever-increasing demand for high performance with maintenance of overall low energy consumption has fuelled the search for new technologies. While it is very challenging to provide optimal levels of robustness against process variability and short channel effects at the nanometre scale, the ultra- thin body and box (UTBB) fully depleted silicon

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Vol-10 Issue-5 No. 9 May 2020

on insulator (FD-SOI) technology has turned out to be a promising candidate for future downscaled transistors [4, 5]

Computers in today's computational era are the basic tool to perform range of functions from simple arithmetic computations to complex artificial intelligence algorithms the fact is that computers are defined by watts not by MIPS (million instruction per seconds). This causes for the need to reduce the heat dissipated which is basically measured in the form power units. Growth of battery based powered systems nowadays increases the issue of controlling the power and keeping a check on it. With the need of user friendly systems designing with features of better mobility, portability, and reliability with simultaneous reduction in cost. In the digital life style, innovation in device structure is another major approach to reduce the power dissipation. IC design space defined previously in terms of speed and area has now been modified in terms of speed, complexity and power [1, 6].

1.1 Silicon on Insulator

The SOI MOSFET (silicon on insulator Metal oxide semiconductor field effect transistor) is an integral part of the modern day IC technology. It takes an important role in the energy conduction and conversion topologies. The threshold voltage (Vth) is an important parameter, which affects the MOSFET characteristics and the noise tolerance ability. It is known about the relationship between Vth and the charges (including fixed charge and traps in the gate oxide and the interface charges at the oxide-si interface) are important parameter. There are literatures about Vth of the short channel MOSFETs and related effects. The influence of the doping profile on Vth has been studied and presented beforehand [6].

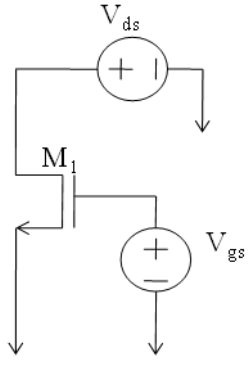

Figure 1.1 MOS without Bulk Bias

1.2 Threshold voltage of MOSFET

Threshold voltage Vth of MOSFETs is defined as the gate bias voltage when the devices are operated in the strong inversion mode. It is mean that the potential of surface is two times the potential of substrate.

Threshold voltage is the minimum voltage applied between the gate and the substrate terminal and is abbreviated as Vgs. It is the minimum voltage needed to make the conducting path between the source and the drain. Here we will use the Vth as abbreviated for the threshold voltage. Vth is the important factor in scaling of power efficiency.

$$Vgs < Vth \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(Eq.1.1)}$$

For the above condition the mosfet will not conduct. Mosfet will be in the off condition to conduct the transistor it is must that Vgs should be equal to or greater then threshold voltage.

$$Vgs \geq Vth \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{(Eq.1.2)}$$

If we focussed on the threshold voltage equation than we can find a solution to reduce threshold voltage.

$$Vth = V_{t0} + \Upsilon ((\sqrt{}(2Øs + Vsb)) - \sqrt{}2Øs) \ldots\ldots\ldots\ldots\ldots \text{(Eq.1.3)}$$

Where Vt0 is the threshold voltage when the source is at the body potential, Øs is the surface potential at threshold, and Υ is the body effect coefficient [7].

1.3 Role of Body Bias

$$Vth = V_{t0} + \Upsilon ((\sqrt{}(2Øs + Vsb)) - \sqrt{}2Øs) \ldots\ldots\ldots\ldots\ldots \text{(Eq.2.1)}$$

According to the above equation it shows that incremental change in Vsb will give rise to the incremental change in the Vth, which in turn will give the incremental change in the drain current even though the gate voltage have been kept constant this shows that body voltage controls the drain current, thus body act as a second gate or an additional control terminal for the MOSFET [8].

2. Low voltage Design Applications

Extremely small current and low supply voltage find applications in biomedical engineering and mobile communication. At low voltage, the major constraint faced is the device noise level. Reduction in VT is dependent on the device technology employed. Higher VT gives better noise immunity and the lower VT reduces the noise margin to result in poor SNR. Hence, for present day CMOS technology, reduction in VT is limited to the noise floor level, below which further reduction will introduce an amount of noise sufficient to result in very complex circuits. Use of low voltage high performing building blocks in low voltage analog circuits is another promising approach and yields a modular design concept in analog circuits as well [9, 10].

ISSN: 2278-4632
Vol-10 Issue-5 No. 9 May 2020

3. Bulk Driven MOSFET

The concept of bulk driven MOSFET was given initially by Blalock et. Al. [11]. One of the most important factor concerning analog and digital circuits is the threshold voltages of standard CMOS technology is not expected to decrease much below what is in demand with the trending technological advancements. The equation of threshold voltage for a practical MOS structure is presented in literature as

$$Vth = V_{t0} + \Upsilon (\sqrt{(Øs + Vsb)} - \sqrt{Øs}) \quad \text{(Eq.3.1)}$$

Where, $VT0$ is the threshold voltage at zero bulk source voltage, Øs is the Fermi potential, γ is the body effect coefficient

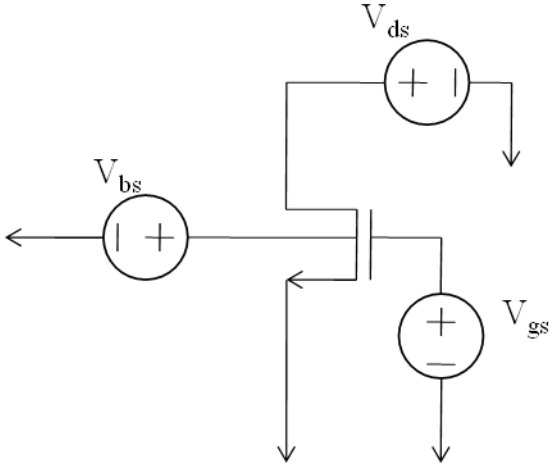

Figure 3.1 MOS with bulk bias

A bulk driven MOSFET has been used to reduce the threshold voltage, it is well known that reverse bias voltage on the well-source junction cause to increase the threshold voltage. Similarly, a forward bias on well- source junction will cause decrease in the threshold voltage. The bulk-driven transistor technique is among one of the techniques for reduction of threshold voltage. Because of the bulk-driven technique MOSFET behaves like a depletion type device, it can operate under zero, negative or even slightly positive biasing condition as shown in fig. 3.1. Where V0 representing the input at the bulk of MOST and Vbs representing the biasing at the gate of MOSFET [12].

The bulk-driven MOSFET operation is much like a JFET. To operate bulk-driven MOSFET, firstly the gate is biased to create a conduction channel of inversion layer by biasing the gate terminal to a fixed voltage that is sufficient to create an inversion layer. This inversion layer gives similar phenomenon similar to a JFET conduction channel by applying a potential difference between drain and source. Since the thickness of the depletion region associated with the conduction channel or inversion layer is affected by the bulk voltage, so by varying the bulk voltage through the body effect of the MOSFET can be modulated the drain current [8, 13].

3.1 Inverter gate driven

As inverter is the basic cell for all digital design systems. Fig. 3.2 is showing the CMOS inverter, comprising of the combination of PMOS and NMOS connecting between supply voltage and ground. Input voltage is applied at the gate of the PMOS and the NMOS transistor. When the applied input signal is low (0V), NMOS gets off and PMOS gets on due to which a path between Vdd and Vout exists. Which results in high output voltage. Similarly, when the applied input voltage is high (Vdd), NMOS gets on, whereas PMOS will gets off due to which a direct path will exists between Vout and the ground, which results in low input voltage. The functionality shown above works as the inverter.

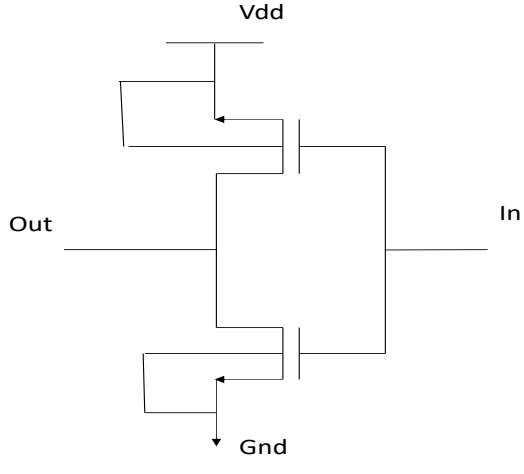

Figure 3.2 Schematic of gate driven inverter

3.2 Inverter bulk driven

Fig.1.4 showing the bulk driven CMOS inverter in which both the MOSFET is used as a four terminal device. The back gate forward body-bias method shown in fig. 3.3 is compatible with CMOS processes. Without any technology modification, the threshold voltage can be removed electrically. When fixed the gate to source voltage (Vin>VT) to off the PMOS and to sufficiently create conducting channel of NMOS and apply signal to the bulk of NMOS (Vbn) this will affect thickness of depletion region associated with inversion layer. Due to this technique

ISSN: 2278-4632
Vol-10 Issue-5 No. 9 May 2020

it will reduce the operating time of NMOS i.e. reduces the threshold voltage of NMOS and produces the output at low supply voltage (i.e.0.7V). Similarly, fixed the gate to source voltage (Vin<VT) to off the NMOS and to sufficiently create conducting channel of PMOS and apply signal to the bulk of PMOS (Vbp) this will affect thickness of depletion region associated with inversion layer. Due to this technique it will reduce the operating time of PMOS i.e. reduces the threshold voltage of PMOS and produces the output at low supply voltage (i.e.0.7V). So bulk driven technique reduces the supply voltage power dissipation of CMOS inverter.

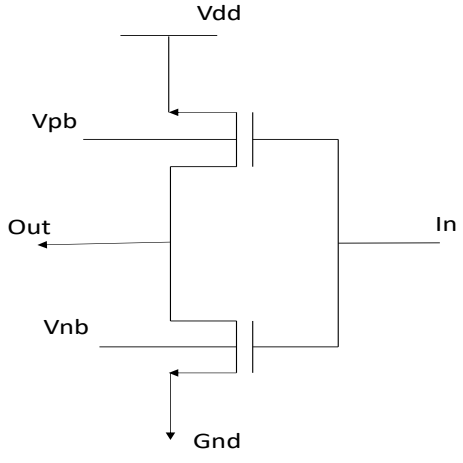

Figure 3.3 Schematic of Bulk Driven inverter

4 Current mirror designs using MOSFET

4.1 Gate driven Current mirror

Current mirror can be used as the basic building blocks in both analog and mixed mode VLSI circuits. A very high input voltages is required for all high impedance CMs to operate them, due to which high output voltage swing can be managed by these current mirrors. The threshold voltage (V) of the input MOSFET decides the requirement of the input voltage, thus CMs are unsuitable for very low voltage operations. Low voltages CM (LVCM) circuits are the need of the hour. Therefore, need to be investigated for getting high voltage swings at the both input and output terminals. A few CM topologies are discussed in [4,5] with reduced input voltage requirements, where they have used either a level shifter or a bulk-driven approaches. The CM proposed in the paper is capable of operating at a supply voltage of 0.7 V.

A new approach to the current mirror for low-voltage CMOS analog signal processing circuits has been developed. In resent days current mirrors only contains gate to drain, or diode connections. Due to this connections the voltage drop is always greater than lV. The bulk-driven current mirror that we have presented in this paper instead utilizes a bulk to drain connection to avoid the large voltage-drop penalty. As a result, for low power applications these current mirrors are well suited. A NMOS erosion of the bulk-driven current mirror is shown in Figure 4.2. Note that instead of the gate-drain diode connection used in the standard simple current mirror, the current mirror used here has a bulk-drain connection. Also, the bulks of M1 and M2 are connected together not the gate terminals. Instead, the gates of M1 and M2 for the NMOS we connected it to the most positive fixed voltage available, VDD. The voltage potential between the gate and source must be greater than or equal to l V in order to form an inversion layer. The NMOS bulk-driven current mirror can be implemented in CMOS p-well technology. To derive an expression for the output current for the simple current mirror shown in Figure 4.1, first consider the mode of operation for each device. M1, the input device, is operated in its linear region. This condition is imposed by MI'S bulk drain connection, forcing Vs=lV. Note that VBSl is positive and that VBSl = VBS2. Ml and M2 reside in the same well and both have source-bulk junctions only slightly forward-biased, provided that aspect ratios have been chosen appropriately for strong inversion operation. It is desirable to only slightly forward-bias the source-bulk junction as it insures that the bulk current remains negligible. If this were not the case, some input current to the mirror circuit would be lost through the bulk. For the bulk-driven current mirror the M1 is operated linearly since VDS1 will be less than VDS2. Note however that M2's drain-source voltage is allowed to exceed VDS, thereby permitting saturation operation [16].

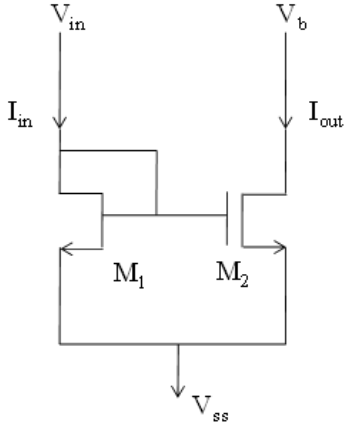

Figure 4.1 Schematic of gate driven current mirror

4.1.1 Input Current range

The CM output produces the accurate current at the output only when the total input current will lie in the range where both the transistors (Ml and M2 in Fig. 4.1) operates in saturation region.

4.1.2 Output voltage Range

An ideal CM produces an accurate output current regardless of the voltage present at the output. In real world minimum voltage must be

ISSN: 2278-4632
Vol-10 Issue-5 No. 9 May 2020

required at the output of the CM to ensure that the devices must operate in saturation region. This voltage is called the output compliance voltage. For a simple current mirror (Fig. 4.1) minimum voltage required is the saturation voltage of the MOSFET2 VDS2 (sat). The output compliance voltage may be differ according to the configuration of the current mirror.

4.1.3 DC Voltage

The drain to source voltage of the current mirror. The transistors MI and M2 (Fig. 4.1) will affects the quality of the current at the output of the mirror. The mismatch error in drain to source voltages is equal to (VDS2- VDSI). This indicates that it will allows the offset current in the current mirror if the drain to source voltages of the mirroring transistors are not balanced.

4.1.4 Dynamic range

The dynamic range for any circuit can be defined as the ratio of maximum signal level to the minimum detectable signal level. The maximum applied signal cab be determined by the input linear range and the noise level at the input of the circuit determines the minimum detectable signal.

4.2 Bulk driven current mirror

This bulk-driven current mirror is capable of operating at threshold voltages within the range of +0.8V and power supplies down to 1V.The requirement for the input voltage to be VGS > VT is removed in this bulk-driven MOSFET configuration. In this paper the operation of the current mirror and first order models of the bulk-driven MOSFET is represented along with the experimental results and the paper also explains the operation of the simple bulk-driven current mirror. The operation of bulk-driven MOSFET is almost same as a JFET. If we connect the gate terminal to a fixed voltage of sufficient magnitude, it will establish the inversion layer which will form the conduction channel beneath to form a channel. The MOSFETs inversion layer beneath the gate structure is the conduction channel of JFET. The bulk potential determines the thickness of the inversion layer, drain and the depletion of the layer beneath the source of the MOSFET. The depletion layer thickness changes by varying the bulk-source voltage, and the inversion layer is modulated through which the drain current is flowing. The channel current can be modulated by a bulk-source potential even if it has a very small dc values. And this results in a device that is very useful for low voltage applications. The current mirrors present days contains the gate-drain or diode connections and for the strong inversion saturation operation, the voltage drop across this connection is greater than | VT |. To keep away from the extensive voltage drop penalty, the bulk driven current mirror is talked about in this paper. Figure 4.2, is showing bulk-driven current mirror. In this, the gate-drain diode connections in the simple current mirror is not used instead of that the bulk-drain connection is used. Rather than the gates, the bulks of transistors M1 and M2 are connected together. The gates of M1 and M2 is connected to the most positive fixed voltage available, VDD. To form the inversion layer beneath the gate, the voltage potential must be greater than or equal to 1V between gate and the source. These NMOS version current mirrors are suitable for low power supply voltage applications.

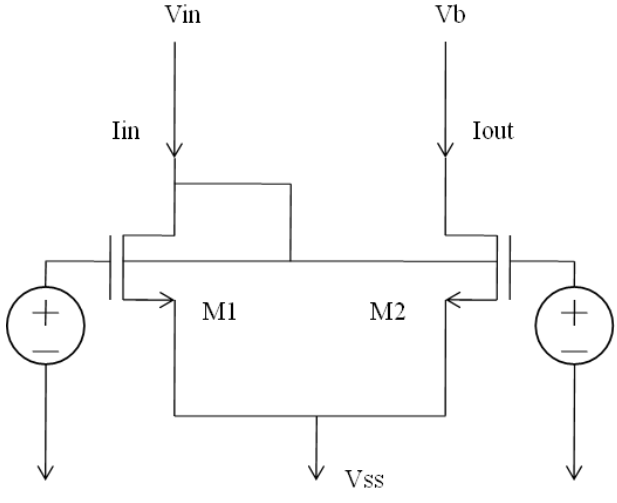

Figure 4.2 bulk driven current mirror

[1]Current mirror is basic block used in analog and mixed mode signal systems for the amplification of current. It is also basically used for the biasing and as an active load for differential amplifiers, nevertheless it converts differential input signal into a single ended output signal. It has high impedance output node. Even if there is variation in load, output current of current mirror remains constant.

Input and output current linearity of gate-driven current mirror is good as both transistors are operated in strong saturation region. However, in this topology, an input voltage (VGS) must be greater or equal to threshold voltage (VT) to switch-on the input transistor. Thus one VT drop occurs in the signal path. If we apply input signal at the bulk of the MOSFET rather than the gate terminal, then NMOS transistor can even switch-on with zero or negative gate-to-source voltage (VGS). Thus additional threshold voltage will not be required at the signal path. This technique thus helps to design low-voltage CMOS circuits. This method can also be used to design low-voltage current mirror, where we can apply input at the bulk terminal of the transistors in the current mirror. Thus this configuration can work at lower supply voltage when compared to the gate-driven. In recent years, several bulk-driven current mirror architectures are presented and Analysed by the researchers.

ISSN: 2278-4632
Vol-10 Issue-5 No. 9 May 2020

For a current mirror the input current and output characteristics show a linear relation with respect to each other. This validates the basic concept of a current mirror circuit that output current characteristics replicate the input characteristics.

ISSN: 2278-4632
Vol-10 Issue-5 No. 9 May 2020

5. Results and observations

The simulations were performed on Cadence Virtuoso Tool on 180nm technology. In this section, we have made a brief discussion on the simulated results of the proposed and the conventional designs.

5.1 DC analysis:

5.1.1 NMOS configuration:

Configuration of basic NMOS with Gate driven and Bulk Driven approach were simulated and corresponding waveforms were obtained.

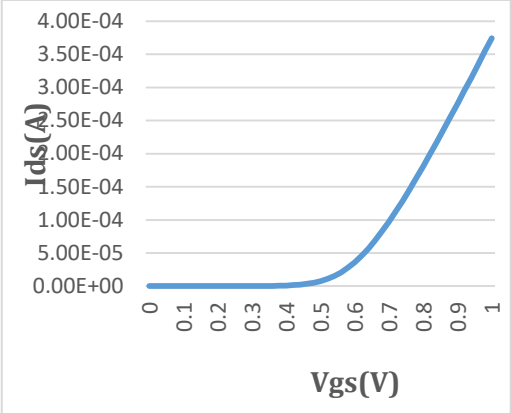

Figure 5.1 Ids vs. Vgs characteristics

Figure 5.1 showing N-MOSFET characteristics in a standard configuration with bulk connected to the source minimum supply voltage. This leads to normal operation of N- MOSFET which depicts the standard characteristics of Ids and Vgs characteristics.

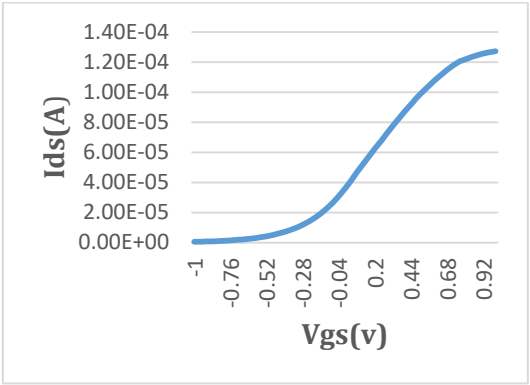

Figure 5.2 Ids vs. Vgs characteristics

Figure 5.2 showing N-MOSFET characteristics in a standard configuration with bulk connected to the source minimum supply voltage. This leads to normal operation of N- MOSFET which depicts the standard characteristics of Ids and Vgs characteristics.

5.1.2 Comparative Study:

Parameters	Bulk MOS	SoI MOS	References	Observation
Supply voltage	Can be Reduced	Can be reduced	1. Hong Ge Li, HuiXinBai, ShuGuoXie, Dong Lin Su, IEEE transactions on electromagnetic compatibility, 2015. 2. Yunxiang yang, Back-Gate Bias dependence of the statistical variability of fdsoi mosfet with thin box. 3. Chris Toumazou, A Low Voltage Bulk Driven Down conversion Mixer Core.	Bulk MOS can work at lower voltage than SOI MOS
Threshold voltage	Can be Varied(INC/DEC)	constant	1.Yasutaka Haga, Izzet Kale ,IEEE,2015 2. Abdolreza Esmaeli, comparison of bulk driven, is floating gate and sub threshold methods in designing of amplifier. 3. Rui He, Evaluation of modern MOSFET models for bulk-driven applications.	Bulk driven approach can minimise the Threshold voltage
Power dissipation	Can be Reduced	Can be reduced applying different technologies	1.Matej Rak, Viera Stopjakov, Arbet Daniel , IEEE,2016 2. Chris Toumazou, A Low Voltage Bulk Driven Down conversion Mixer Core. 3. Yasutaka Haga, Bulk-Driven Flipped Voltage Follower.	Power dissipation can be reduced to much extent in bulk MOS
Mixed Mode Circuits Application	Better	Can be used	1.Lukas Nagy, Daniel Arbet, Martin Kovac and Vieira Stopjakova, IEEE Africon Proceedings 2017	Mixed mode circuits can operate at low supply voltage

ISSN: 2278-4632
Vol-10 Issue-5 No. 9 May 2020

			2. Matej rak, analyse the bulk driven technique to operate low voltage IC designs in 130nm CMOS technology. 3. Montree kumngern, shows the 0.5v fully differential current conveyor using bulk driven quasi floating gate technique.	using Bulk MOS
Low power Analog devices Application	Better	Can be used	1.Montree kumngern,f abian khateb, IET Circuits, Devises & Systems 2016 2. Yasutaka haga, Bulk Driven DC level shifter. 3. Yasutaka Haga, Bulk-Driven Flipped Voltage Follower.	Analog devices works at low voltage using Bulk MOS

Body terminal voltage of the MOSFET is usually called as the source of error in some cases. We must care about the bulk terminal in using it as the second gate or in applying input to it and this will provide the signal amplification in this condition also. From the above discussion it is clear that the body source voltage can affect the threshold voltage. As shown in Figure 5.1 the Ids vs. Vgs characteristics of Bulk MOS and SOI MOS which is simply showing the threshold voltage of bulk MOS can be reduced much more than SOI MOS due to increase of the body terminal voltage with respect to the source.

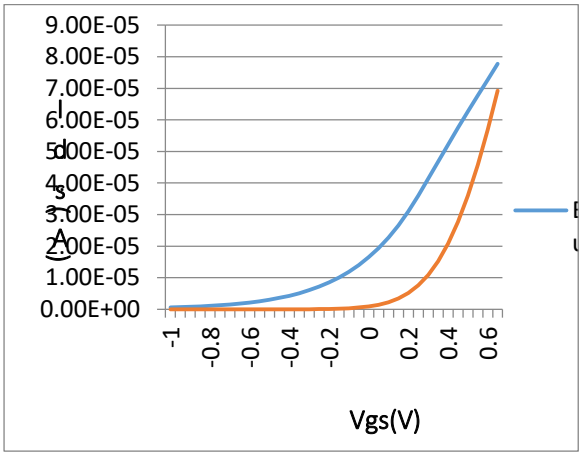

Figure 5.3 comparative Ids vs. Vgs characteristics

5.2.3 Transient analysis:

Figure 5.4 and 5.5 showing the input - output characteristics of the gate driven and bulk driven inverter respectively. For the low input the inverter gives the high output.

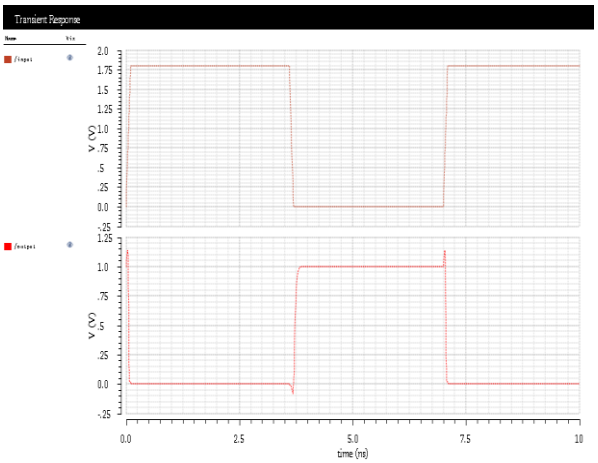

Figure 5.4 input output characteristics of gate driven inverter

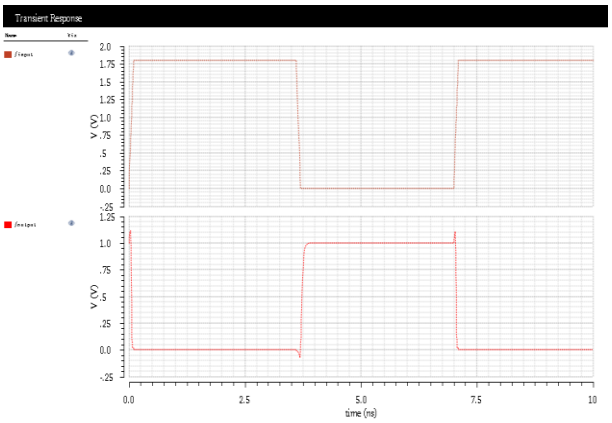

Figure 5.5 input output characteristics of bulk driven inverter

5.2.4 DC analysis:

Figure 5.6 and 5.7 showing the voltage transfer characteristics of the gate driven and bulk driven inverter respectively. At different Vds we have calculated the voltage transfer characteristics for both the gate.

ISSN: 2278-4632
Vol-10 Issue-5 No. 9 May 2020

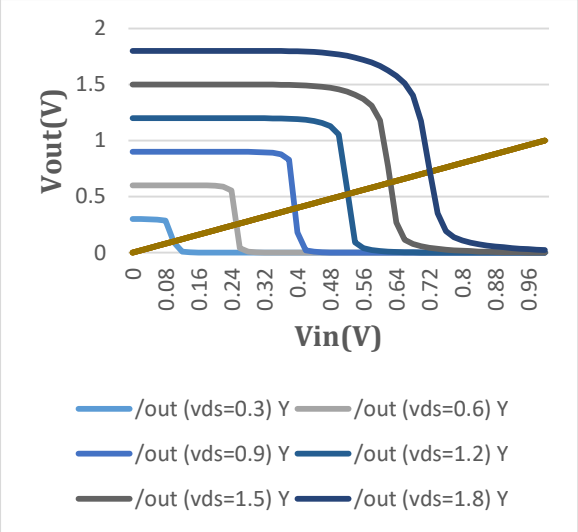

Figure 5.6 Voltage transfer characteristics of Bulk driven inverter

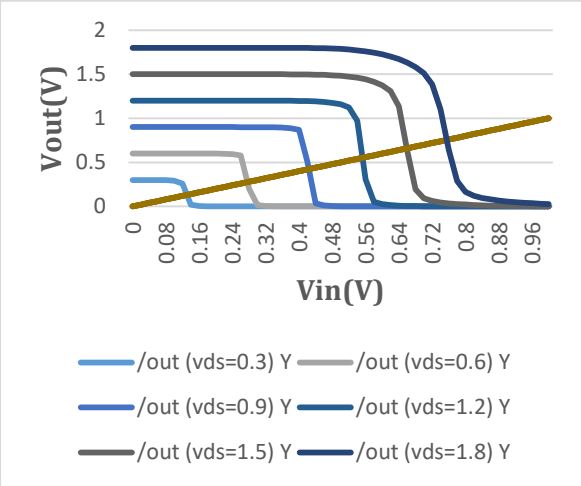

Figure 5.7 Voltage transfer characteristics of gate driven inverter

5.3 Comparative study

{2}To study the threshold voltage and the others characteristics parameters of the inverter such as noise margin, area of operation of the MOSFET etc. one has to draw the voltage transfer characteristics if the inverter. Voltage transfer characteristics and to calculate threshold voltage is the main issue for designer Figure 5.8 represents the voltage transfer characteristics of both gate driven and bulk driven inverter. The switching threshold voltage of the inverter can be calculated from the given below characteristics where the input voltage is equal to the output voltage and both the transistor works in the saturation region.

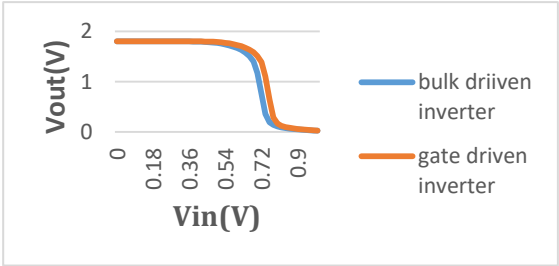

Figure 5.8 comparative studies of bulk and gate driven inverter

Circuit	Supply voltage(V)	Wp/L	Wn/L	Propagation delay (ns)	Figure of Merit	Noise margin	Threshold voltage(V)
GATE DRIVEN INVERTER	1.8	4/.18	2/.18	0.125	6.325	0.73	0.76
BULK DRIVEN INVERTER	1.8	4/.18	2/.18	0.103	5.085	0.57	0.72

ISSN: 2278-4632
Vol-10 Issue-5 No. 9 May 2020

5.4 Gate driven current mirror configuration:

5.4.1 Power supply voltage Vdd vs. output current:

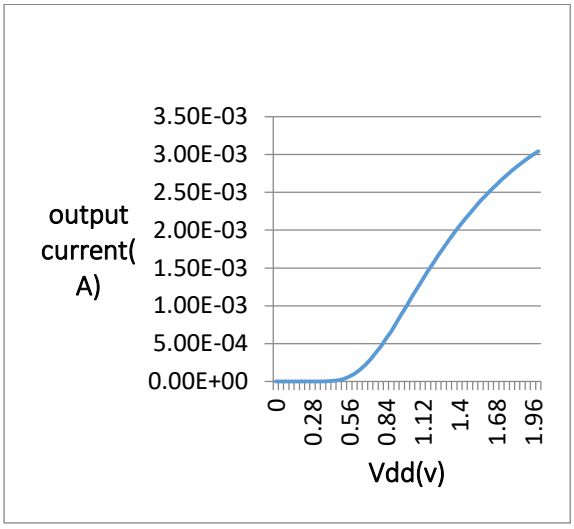

Figure 5.9 input voltage vs. Output current characteristics

{3}The above Simulation results shows the output current under different supply voltages to check the requirement of the bias voltage (Fig. 5.9). To achieve less than 1000µA currents, the circuit is performing satisfactory at a single supply voltage of 1V.

5.4.2 Input voltage vs. input current:

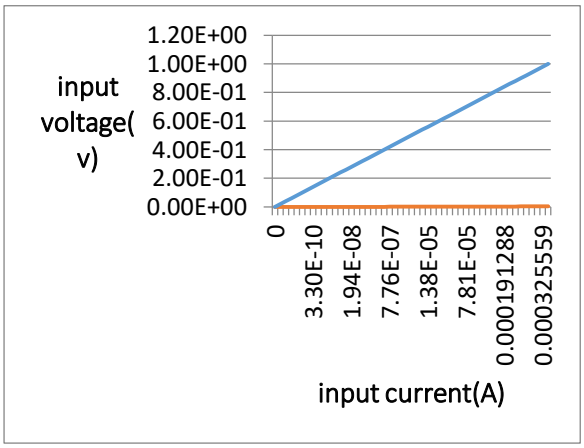

Figure 5.10 input voltage vs. Input current characteristics

For Iin, between lnA and 305µA. Input voltage (Vin) is plotted in Fig. 5.10 for different values of input voltage. Vin required is 1V for 305µA of Iout. This voltage is still higher to operate CM for low voltage applications.

5.4.3 Input current vs. output current:

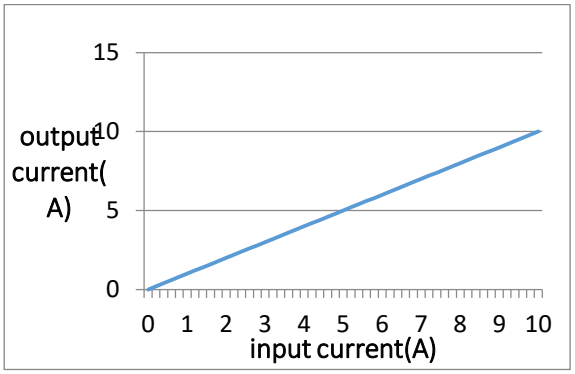

Figure 5.11 input current vs. Output current characteristics

The above characteristics shows the input current vs. output current of the gate driven current mirror. From above it is clear that the output current follows the same as the input current.

5.4.4 Bias voltage vs. output current:

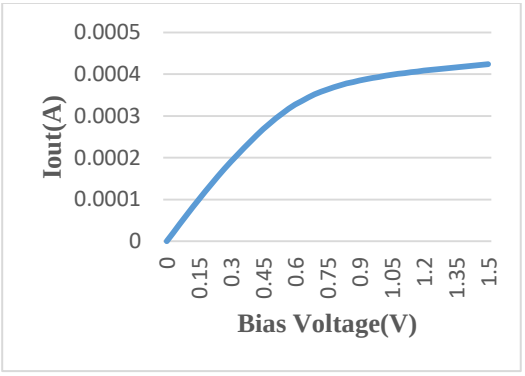

Figure 5.12 output current vs. Bias voltage characteristics

We find that V, is 1V for Iin, of 305µA for gate driven current mirror. Fig. 5.12 showing the plot of bias voltage vs. Iout. It requires an output voltage less than 0.6V for I, up to 300µA and approximately 1V for I, greater than 400µA.

5.4.5 Power supply voltage Vdd vs. output current:

ISSN: 2278-4632
Vol-10 Issue-5 No. 9 May 2020

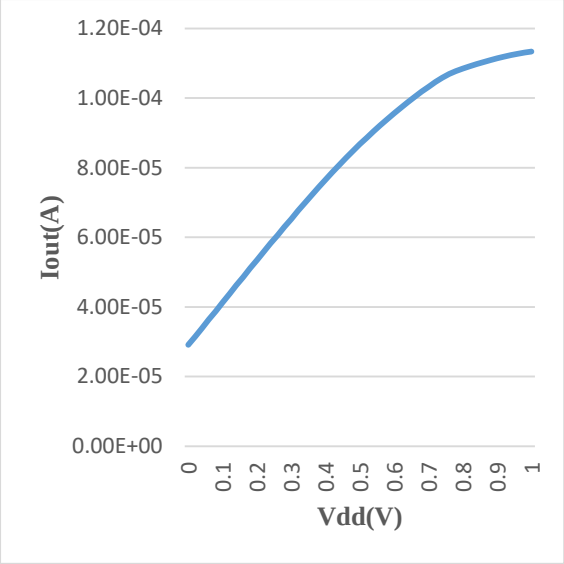

Figure 5.13 Vdd vs. Iout

The above Simulation results shows the output current under different supply voltages to check the requirement of the bias voltage (Fig. 5.13). To achieve less than 100µA currents, the circuit is performing satisfactory at a single supply voltage of 1V.

5.4.6 Input current vs. output current:

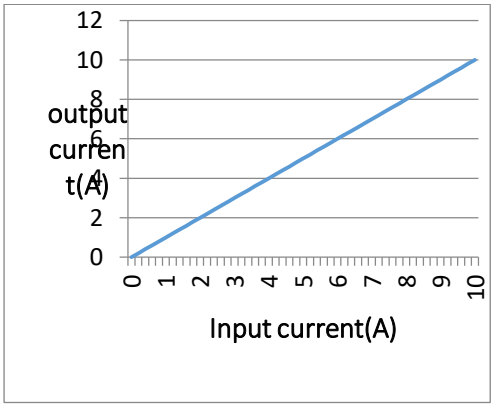

Figure 5.14 input current vs. output current

The above characteristics shows the input current vs. output current of the gate driven current mirror. From above it is clear that the output current follows same as the input current as the principle of a. Basic current mirror circuit.

5.4.7 Input current vs. output current:

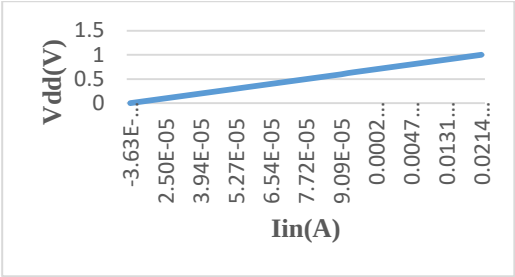

Figure 5.15 Iin vs. Vdd

For Iin, between lnA and 2000µA. Input voltage (Vin) is plotted in Fig. 5.15 for different values of input voltage. Vin required is 1V for 2000µA of Iout. In comparision to the gate driven current mirror only 0.7v is required for low voltage bulk driven CM.

5.4.8 Bias voltage vs. output current:

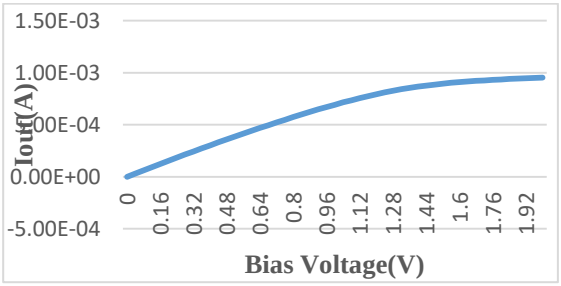

Figure 5.16 Bias voltage vs. Iout

We find that V, is 1V for Iin, of 700µA for bulk driven current mirror. Fig. 5.16 Is the plot of bias voltage against Iout. This requires an output voltage which is clearly visible that it is less than 0.4V for I, up to 300µA and approximately 1V for I, greater than 700µA.

ISSN: 2278-4632
Vol-10 Issue-5 No. 9 May 2020

5.5 Comparative study:

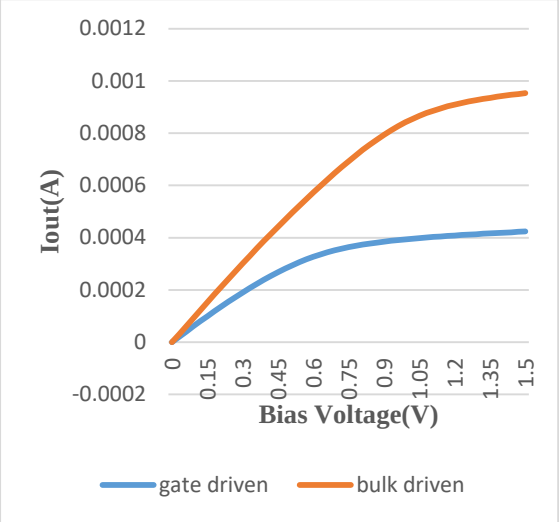

Figure 5.17 Bias Voltage vs. Iout

Parameters	Gate Driven Current Mirror	Bulk Driven Current Mirror
Technology(µm)	0.18	0.18
Supply Voltage(V)	1	0.7
Current Range(µA)	0-400	0-900
Offset Error (%)	0.012	0.02
Input Resistance(kΩ)	1	1
Output Resistance(kΩ)	1	1
Minimum Output Voltage(V)	0.54	0.31

From the comparative analysis done for the MOSFET based current mirror circuits. It's clearly showing that low supply voltage leading to low threshold voltage is successfully implemented with respect to low power design.

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